REIDITE INDUSTRIES

ACRIX Series

Datasheet

Open-frame (ACRIX-A1)

Phantom Forge® encapsulated (ACRIX-A2)

v1.0

June 29, 2026

Company:	REIDITE Industries
Document:	ACRIX Datasheet
Status:	Release v1.0 – Distribution

1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2026-06-19	Release 1.0 for distribution.

2 Hardware version guide

This documentation applies to ACRIX hardware version **1.1.0**. Ensure that your module and carrier design match this revision; for other hardware versions, contact REIDITE Industries or refer to the ACRIX product page (downloads).

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3 Introduction

The ACRIX A1/A2 are a series of System-On-Module (SoM) devices aimed at control, communications, and signal processing applications for demanding environments. Thanks to it's patented technology Phantom Forge®the system can sustain up to 140ºC of temperature and meets IP66 rating for particle and water resistance. This SoM embeds a powerful MCU coupled with an FPGA for industrial scenarios where power efficency, flexibility and reliability are key aspects.

The family is designed to scale across performance and protection classes while maintaining a consistent software and electrical interface, simplifying reuse across product lines and reducing time to qualification.

3.1 Key features

- Hybrid MCU STM32H563ZIT6 + ICE40UP5K architecture.
- Secure boot and remote update support (optional).
- Extended industrial temperature range (variant dependent).
- Deterministic timing and configurable data paths via FPGA logic.
- Consistent pinout and software baseline across the family.
- Supported RTOS: FreeRTOS.
- Rich MCU GPIO:
  - 15 proprietary GPIO pins
  - 29 x FPGA GPIO Pins
  - 1 x RMII Ethernet up to 100MB/s
  - 2 x UART
  - 2 x CAN
  - 3 x I²C
  - 3 x SPI
  - 1 x OctoSPI
  - 1 x USB 2.0 (High Speed)
  - 1 x SDMMC
- Small footprint 55 mm × 40 mm (without encapsulation); 57,6mm × 42,6mm (with encapsulation)
- 4 x M2.2 mounting holes
- **RoHS free** (all variants).

4 Interfaces

4.1 Power Monitoring

The SoM integrates an INA226AQ chip for real-time measurmente of current, voltage and power consumption. This chip is directly communicated to the main MCU STM32H563ZIT6 through an I²C interface.

- Bus voltage monitoring
- Current sensing
- Power calculation
- Programmable alert functionality
- High-side current measurement

4.2 USB 2.0

Integration of USB 2.0 interface through the USB controller of the STM32H563ZIT6 microcontroller. The USB interface signals are routed to the module connector for implementation on an external carrier board.

Signal Name	Description
USB_VBUS	USB bus voltage detection
USB_ID	USB OTG identification signal
USB_DP	USB differential data positive
USB_DN	USB differential data negative

Table 1: Exposed USB Signals

4.2.1 Features

- USB 2.0 compliant interface
- USB OTG support
- Integrated USB controller in STM32H563ZIT6

4.3 ACRIX GPIO Interface

The board exposes 15 general-purpose input/output (GPIO) signals provided by the STM32H563ZIT6 microcontroller to the module connector. GPIO signals operate at 3.3 V logic levels and are not 5 V tolerant unless explicitly stated in the STM32H563ZIT6 datasheet. Each GPIO can be configured by firmware as:

- Digital input
- Digital output
- External interrupt source
- Alternate peripheral function

4.3.1 Features:

- 3.3 V CMOS logic levels

- Firmware-configurable direction and function
- Internal pull-up and pull-down resistor configuration
- External interrupt capability on supported pins
- Alternate peripheral functions depending on pin assignment

4.3.2 FPGA GPIO Interface

The board exposes 29 user-programmable FPGA I/O signals from the Lattice iCE40 FPGA to the module connector. These signals may be configured through FPGA configuration to implement custom digital interfaces and logic functions.

4.3.3 Features:

- User-programmable FPGA I/O
- Direct FPGA fabric connectivity
- Custom digital interface implementation capability
- FPGA-defined signal functionality

4.4 CAN

The device supports CAN signal routing from the STM32H563ZIT6 microcontroller to the module connector. An external CAN transceiver on the carrier board is required to interface these signals with a physical CAN bus.

Signal Name	Description
CAN2_TX	CAN2 transmit signal from MCU
CAN2_RX	CAN2 receive signal to MCU
CAN3_TX	CAN3 transmit signal from MCU
CAN3_RX	CAN3 receive signal to MCU

Table 2: Exposed CAN Signals

Features:

- STM32 integrated FDCAN controller
- Classic CAN support
- CAN FD support, depending on firmware configuration
- External CAN transceiver required on carrier board

4.5 SPI

The board exposes multiple SPI interfaces for high-speed synchronous serial communication.

Interface	Function
SPI1	External Interface
SPI2	External Interface
SPI4	External Interface

Table 3: Exposed SPI Signals

The SPI interfaces operate at 3.3V logic levels and may be used for communication with external peripherals such as:

- Sensors
- ADC/DAC devices
- Displays
- External controllers
- Memory devices

4.6 FPGA SPI

When the module starts for the first time, the FPGA does not contain any preconfigured firmware. Therefore, the MCU is responsible for uploading the firmware by programming the external flash memory. Once the firmware has been uploaded (and after a hard reset), the FPGA loads and executes the code stored in the flash through the shared SPI communication bus.

This SPI bus is shared between the MCU, the FPGA, and the external flash memory. Although the four communication lines are routed to the FX11 connectors, it is recommended not to use this bus for purposes other than its intended operation.

4.7 I²C

The board exposes multiple I²C interfaces for peripheral communication and system monitoring.

Interface	Function
I²C1	External peripheral expansion
I²C2	External peripheral expansion
I²C4	Internal monitoring and FPGA communication

Table 4: Exposed I²C Signals

I²C4 is used internally for communication between the FPGA subsystem and the INA226 power monitor. All I²C interfaces operate at 3.3V logic levels. External pull-up resistors may be required depending on bus topology and connected peripherals.

5 Electrical & Mechanical

5.1 Electrical specification

This section shows the absolute maximum limits of the system. Values exceeding those in Table 5 may cause permanent damage to the device.

Symbol	Parameter	Minumum	Maximum	Unit
V_{in}	Input Voltage	-0.3	20	V
V_{GPIO_REF}	GPIO Voltage	-0.35	3.6	V
V_{GPIO}	GPIO Input Voltage	-0.35	3.76	V

Table 5: Absolute Maximum Limits

Symbol	Parameter	Conditions	STM32H563	iCE40UP5K	Unit
V_{DD}	Core / I/O supply	Typical GPIO bank supply	1.71–3.6	1.2 core/1.2–3.3 IO	V
V_{IL}	Input low voltage	CMOS input	$\leq$ 0.3 × VDD	$\leq$ 0.3 × VCCIO	V
V_{IH}	Input high voltage	CMOS input	$\geq$ 0.7 × VDD	$\geq$ 0.7 × VCCIO	V
V_{OL}	Output low voltage	IOL max	$\leq$ 0.4	$\leq$ 0.4	V
V_{OH}	Output high voltage	IOH max	$\geq$ VDD – 0.4	$\geq$ VCCIO – 0.4	V
I_{IL}	Input leakage current	GPIO input	$\pm$1	$\pm$10	uA
I_{OH}	Output source current	Per GPIO	~8	~8	mA
I_{OL}	Output sink current	Per GPIO	~8	~8	mA
RPU	Internal pull-up resistor	Typical	30–50	~100	kΩ
RPD	Internal pull-down resistor	Typical	30–50	~100	kΩ
FT	5V tolerant inputs	Selected GPIOs only	Yes	No	-
OD	Open-drain support	GPIO mode	Yes	Via logic / RGB pins native	-
Differential I/O	LVDS support	Differential pairs	Limited	Yes	-
Schmitt Trigger	Input hysteresis	GPIO input	Yes	Limited	-
Slew Control	Configurable output slew	GPIO output	Yes	Yes	-
Drive Strength	Configurable	GPIO output	Yes	Yes	-

Table 6: Recommended DC operating values

Please be aware that the FPGA pins are not 5V tolerant. Nonetheless, most MCU pins are 5V tolerant. Please refer to the respective datasheet for more information regarding pin and power characteristics.

State	Current
Standby	60 mA
Run (MCU)	100 mA
Run (MCU + FPGA)	115 mA

Table 7: Power states (estimated values).

The values in 7 are provided for reference only. Actual power consumption may vary between modules.

5.2 Thermal

ACRIX modules are specified for industrial environments where thermal, mechanical, and electrical stress are higher than in typical commercial applications. All variants support an operating temperature range starting at -40 °C; the upper limit depends on the variant (85 °C for ACRIX-A1, and 140 °C for ACRIX-A2). These limits assume that the module is used within the specified supply and interface conditions and that adequate cooling or thermal coupling is provided when the system runs at high load for extended periods.

5.3 Mechanical

The ACRIX module has a small footprint of 55mm × 40 mm. With the Phantom Forge case, the module measures 57.6mm × 42.6mm. The module features 4 M2.2 holes on each corner for mounting. The PCB thickness is 1.6mm ± 10%. Final height (with components) is 5.6mm. The Figure 1 shows the mechanical drawing of the ACRIX with its most relevant dimensions. All measurements are in mm.

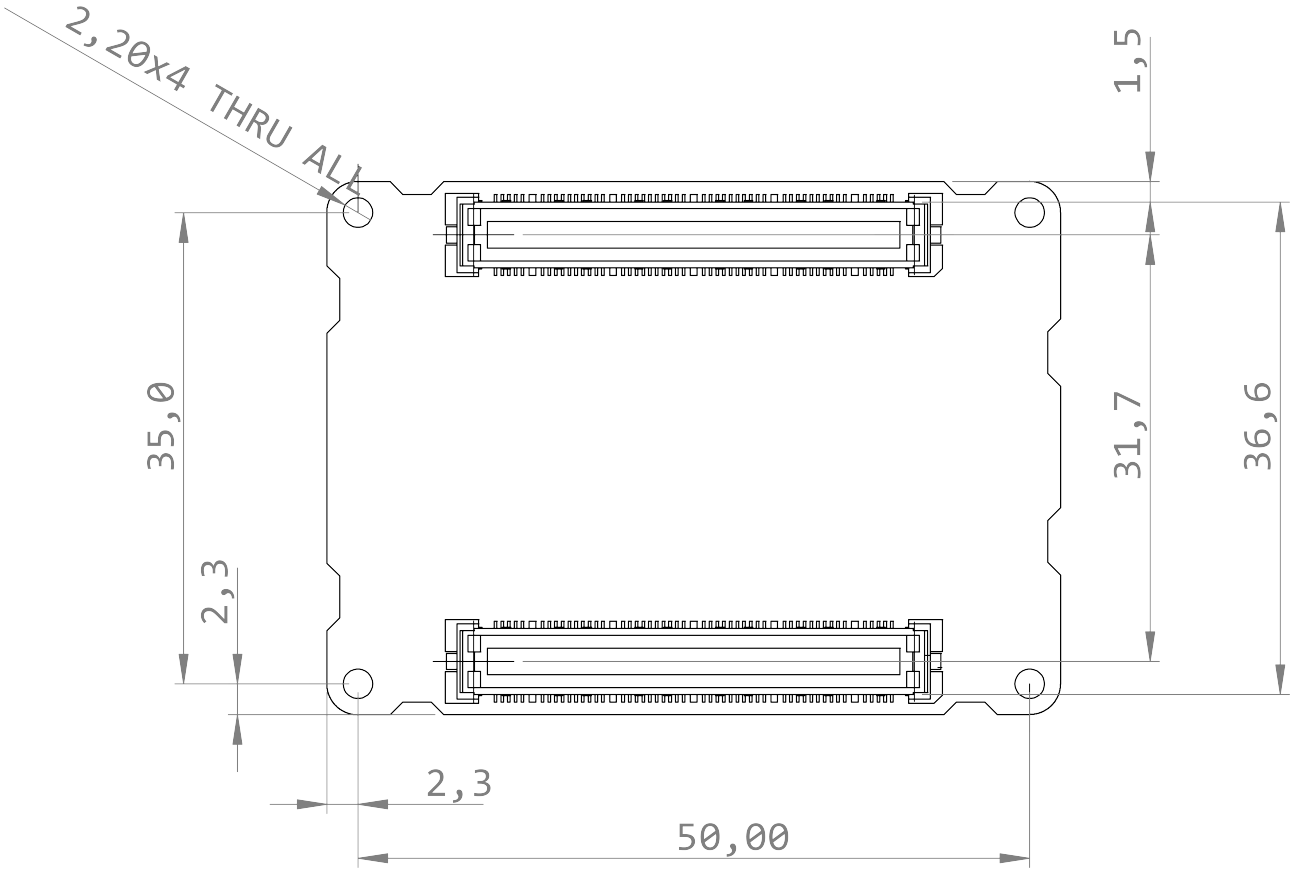

Figure 1: Bottom mechanical drawing of ACRIX

There must be at least 2mm of clearance between the ACRIX and the carrier board for successful mating. For information on the connectors, please refer to the FX11LA-100S/10-SV(92).

6 Pinout

7 Connector pinout

ACRIX exposes I/O through two 100-pin connector strips (J1 and J2), using Hirose FX11LA-100/10. Use the diagram and tables below for carrier-board design. Many signals are multifunction (GPIO, SPI, I^2C, UART, CAN, SDMMC, USB, debug). Pins are not 5 V tolerant unless explicitly stated.[1]

7.1 J1 connector (100 pins)

Pin	Signal	Pin	Signal
J1-001	VDD	J1-002	IOB_8A
J1-003	VDD	J1-004	N.C.
J1-005	GND	J1-006	N.C.
J1-007	USB_DN	J1-008	N.C.
J1-009	USB_DP	J1-010	N.C.
J1-011	VIN	J1-012	IOB_0A
J1-013	VIN	J1-014	IOB_5B
J1-015	GND	J1-016	IOB_3B_G6
J1-017	FPGA_+3V3	J1-018	IOT_49A
J1-019	FPGA_+3V3	J1-020	IOT_51A
J1-021	GND	J1-022	GND
J1-023	FPGA_+1V2	J1-024	#LED_RGB2
J1-025	FPGA_+1V2	J1-026	#LED_RGB1
J1-027	GND	J1-028	#LED_RGB0
J1-029	PWR_ON	J1-030	IOT_50B
J1-031	NRESET	J1-032	IOT_45A_G1
J1-033	GND	J1-034	GND
J1-035	DONE	J1-036	IOT_48B
J1-037	GND	J1-038	IOT_46B_G0
J1-039	N.C.	J1-040	GND
J1-041	GND	J1-042	IOT_44B
J1-043	GPIO_14	J1-044	IOT_43A
J1-045	GPIO_15	J1-046	GND
J1-047	I2C2_SDA	J1-048	IOT_42B
J1-049	I2C2_SCL	J1-050	IOT_41A
J1-051	HDMI_CEC	J1-052	IOT_38B
J1-053	GND	J1-054	IOT_39A
J1-055	GND	J1-056	GND
J1-057	GND	J1-058	IOT_36B
J1-059	N.C.	J1-060	IOT_37A
J1-061	N.C.	J1-062	GND
J1-063	GPIO_11	J1-064	IOT_23B
J1-065	N.C.	J1-066	N.C.

[1] Note: In order for the ACRIX to work please make sure all the GND pins are correctly connected.

Pin	Signal	Pin	Signal
J1-067	SPI4_MOSI	J1-068	N.C.
J1-069	SPI4_MISO	J1-070	GND
J1-071	GPIO_3	J1-072	N.C.
J1-073	SPI4_SCK	J1-074	IOB_33B_SPI_SI
J1-075	SPI1_MOSI	J1-076	GND
J1-077	N.C.	J1-078	IOB_35B_SPI_SS
J1-079	N.C.	J1-080	IOB_34A_SPI_SCK
J1-081	N.C.	J1-082	GND
J1-083	N.C.	J1-084	IOB_32A_SPI_SO
J1-085	N.C.	J1-086	IOB_24A
J1-087	N.C.	J1-088	IOB_22A
J1-089	N.C.	J1-090	IOB_20A
J1-091	SPI2_MOSI	J1-092	IOB_18A
J1-093	SPI2_MISO	J1-094	IOB_16A
J1-095	SPI2_CLK	J1-096	IOB_13A
J1-097	CAN3_RX	J1-098	C_DONE
J1-099	CAN3_TX	J1-100	#C_RESET

7.2 J2 connector (100 pins)

Pin	Signal	Pin	Signal
J2-001	N.C.	J2-002	POWER_EN
J2-003	GND	J2-004	UART7_RX
J2-005	VDD	J2-006	UART7_TX
J2-007	I2C1_SCL	J2-008	BOOT0
J2-009	I2C1_SDA	J2-010	CONN_ERR
J2-011	GPIO_7	J2-012	CONN_ERR
J2-013	SPI1_CLK	J2-014	VIN
J2-015	VDD	J2-016	VIN
J2-017	VDD	J2-018	VIN
J2-019	I2C2_SDA	J2-020	VIN
J2-021	I2C2_SCL	J2-022	VIN
J2-023	VDD	J2-024	VIN
J2-025	SPI1_MISO	J2-026	VDD
J2-027	N.C.	J2-028	#RESET
J2-029	SDMMC1_D6	J2-030	GND
J2-031	SDMMC1_D7	J2-032	SDMMC1_D2
J2-033	SDMMC1_D4	J2-034	SDMMC1_D1
J2-035	GND	J2-036	GND
J2-037	SDMMC1_D5	J2-038	SDMMC1_D0
J2-039	SDMMC1_CMD	J2-040	SDMMC1_D3
J2-041	GND	J2-042	GND
J2-043	GPIO_2	J2-044	SDMMC1_CK
J2-045	GPIO_3	J2-046	GPIO_13
J2-047	GPIO_4	J2-048	GPIO_9
J2-049	GPIO_5	J2-050	GPIO_8

Pin	Signal	Pin	Signal
J2-051	UART8_RX	J2-052	GND
J2-053	UART8_TX	J2-054	DBG_JTMS
J2-055	GND	J2-056	GND
J2-057	CAN2_RX	J2-058	DBG_JTCK
J2-059	CAN2_TX	J2-060	GND
J2-061	GND	J2-062	DBG_JTDO
J2-063	I2C4_SDA	J2-064	GND
J2-065	GND	J2-066	DBG_JTDI
J2-067	I2C4_SCL	J2-068	GND
J2-069	GND	J2-070	DBG_NRST
J2-071	8SPI_P1_IO2	J2-072	8SPI_P1_IO1
J2-073	8SPI_P1_IO3	J2-074	8SPI_P1_IO0
J2-075	8SPI_P1_IO4	J2-076	8SPI_P1_DQS
J2-077	8SPI_P1_IO5	J2-078	8SPI_P1_NCS
J2-079	8SPI_P1_IO6	J2-080	8SPI_P1_CLK
J2-081	8SPI_P1_IO7	J2-082	GND
J2-083	N.C.	J2-084	USB_VBUS
J2-085	N.C.	J2-086	N.C.
J2-087	N.C.	J2-088	USB_CC1
J2-089	N.C.	J2-090	USB_CC2
J2-091	N.C.	J2-092	N.C.
J2-093	N.C.	J2-094	N.C.
J2-095	N.C.	J2-096	N.C.
J2-097	N.C.	J2-098	N.C.
J2-099	GND	J2-100	GND

7.3 Pin description

Pin	Signal	Description
J1-001	VDD	+3V3 ACRIX PMIC Output
J1-002	IOB_8A	FPGA GPIOB 8A
J1-003	VDD	+3V3 ACRIX PMIC Output
J1-004	N.C.	Not Connected
J1-005	GND	Ground (0V)
J1-006	N.C.	Not Connected
J1-007	USB_DN	MCU USB differential data line minus
J1-008	N.C.	Not Connected
J1-009	USB_DP	MCU USB differential data line plus
J1-010	N.C.	Not Connected
J1-011	VIN	+5V main power input
J1-012	IOB_0A	General-purpose FPGA I/O
J1-013	VIN	+5V main power input
J1-014	IOB_5B	General-purpose FPGA I/O
J1-015	GND	Ground (0V)
J1-016	IOB_3B_G6	General-purpose FPGA I/O
J1-017	FPGA_+3V3	+3V3 FPGA output, independent from PMIC +3V3
J1-018	IOT_49A	General-purpose FPGA I/O
J1-019	FPGA_+3V3	+3V3 FPGA output, independent from PMIC +3V3
J1-020	IOT_51A	General-purpose FPGA I/O
J1-021	GND	Ground (0V)
J1-022	GND	Ground (0V)
J1-023	FPGA_+1V2	+1V2 FPGA output
J1-024	#LED_RGB2	LED2 sink / general-purpose FPGA I/O. Active low
J1-025	FPGA_+1V2	+1V2 FPGA output
J1-026	#LED_RGB1	LED1 sink / general-purpose FPGA I/O. Active low
J1-027	GND	Ground (0V)
J1-028	#LED_RGB0	LED0 sink / general-purpose FPGA I/O. Active low
J1-029	PWR_ON	Power-on control signal
J1-030	IOT_50B	General-purpose FPGA I/O
J1-031	NRESET	System reset signal, active low
J1-032	IOT_45A_G1	General-purpose FPGA I/O
J1-033	GND	Ground (0V)
J1-034	GND	Ground (0V)
J1-035	DONE	FPGA configuration done signal. Goes high when FPGA is configured
J1-036	IOT_48B	General-purpose FPGA I/O
J1-037	GND	Ground (0V)
J1-038	IOT_46B_G0	General-purpose FPGA I/O
J1-039	N.C.	Not Connected
J1-040	GND	Ground (0V)
J1-041	GND	Ground (0V)
J1-042	IOT_44B	General-purpose FPGA I/O
J1-043	GPIO_14	General-purpose input / output 14
J1-044	IOT_43A	General-purpose FPGA I/O
J1-045	GPIO_15	General-purpose input / output 15
J1-046	GND	Ground (0V)
J1-047	I2C2_SDA	MCU I2C2 serial data, bidirectional, open-drain with pull-up

Pin	Signal	Description
J1-048	IOT_42B	General-purpose FPGA I/O
J1-049	I2C2_SCL	MCU I2C2 serial clock, open-drain with pull-up
J1-050	IOT_41A	General-purpose FPGA I/O
J1-051	HDMI_CEC	HDMI Consumer Electronics Control signal
J1-052	IOT_38B	General-purpose FPGA I/O
J1-053	GND	Ground (0V)
J1-054	IOT_39A	General-purpose FPGA I/O
J1-055	GND	Ground (0V)
J1-056	GND	Ground (0V)
J1-057	GND	Ground (0V)
J1-058	IOT_36B	General-purpose FPGA I/O
J1-059	N.C.	Not Connected
J1-060	IOT_37A	General-purpose FPGA I/O
J1-061	N.C.	Not Connected
J1-062	GND	Ground (0V)
J1-063	GPIO_11	General-purpose input / output 11
J1-064	IOT_23B	General-purpose FPGA I/O
J1-065	N.C.	Not Connected
J1-066	N.C.	Not Connected
J1-067	SPI4_MOSI	MCU SPI4 master output / slave input
J1-068	N.C.	Not Connected
J1-069	SPI4_MISO	MCU SPI4 master input / slave output
J1-070	GND	Ground (0V)
J1-071	GPIO_3	General-purpose input / output 3
J1-072	N.C.	Not Connected
J1-073	SPI4_SCK	MCU SPI4 serial clock
J1-074	IOB_33B_SPI_SI	FPGA SPI serial input / general-purpose FPGA I/O
J1-075	SPI1_MOSI	MCU SPI1 master output / slave input
J1-076	GND	Ground (0V)
J1-077	N.C.	Not Connected
J1-078	IOB_35B_SPI_SS	FPGA SPI slave select / general-purpose FPGA I/O
J1-079	N.C.	Not Connected
J1-080	IOB_34A_SPI_SCK	FPGA SPI serial clock / general-purpose FPGA I/O
J1-081	N.C.	Not Connected
J1-082	GND	Ground (0V)
J1-083	N.C.	Not Connected
J1-084	IOB_32A_SPI_SO	FPGA SPI serial output / general-purpose FPGA I/O
J1-085	N.C.	Not Connected
J1-086	IOB_24A	General-purpose FPGA I/O
J1-087	N.C.	Not Connected
J1-088	IOB_22A	General-purpose FPGA I/O
J1-089	N.C.	Not Connected
J1-090	IOB_20A	General-purpose FPGA I/O
J1-091	SPI2_MOSI	MCU SPI2 master output / slave input
J1-092	IOB_18A	General-purpose FPGA I/O
J1-093	SPI2_MISO	MCU SPI2 master input / slave output
J1-094	IOB_16A	General-purpose FPGA I/O
J1-095	SPI2_CLK	MCU SPI2 clock
J1-096	IOB_13A	General-purpose FPGA I/O
J1-097	CAN3_RX	MCU CAN3 receiver

Pin	Signal	Description
J1-098	C_DONE	FPGA configuration done signal
J1-099	CAN3_TX	MCU CAN3 transmitter
J1-100	#C_RESET	FPGA reset signal, active low
J2-001	N.C.	Not Connected
J2-002	POWER_EN	Enable pin for internal PMIC
J2-003	GND	Ground (0V)
J2-004	UART7_RX	MCU UART7 receiver
J2-005	VDD	+3V3 ACRIX output
J2-006	UART7_TX	MCU UART7 transmitter
J2-007	I2C1_SCL	MCU I2C1 serial clock, open-drain with pull-up
J2-008	BOOT0	MCU boot mode selection input
J2-009	I2C1_SDA	MCU I2C1 serial data, bidirectional, open-drain with pull-up
J2-010	CONN_ERR	Pin for ensuring correct placement of ACRIX in the carrier board. Do not connect anything to this pin
J2-011	GPIO_7	General-purpose input / output 7
J2-012	CONN_ERR	Pin for ensuring correct placement of ACRIX in the carrier board. Do not connect anything to this pin
J2-013	SPI1_CLK	MCU SPI1 serial clock
J2-014	VIN	+5V main power input
J2-015	VDD	+3V3 ACRIX output
J2-016	VIN	+5V main power input
J2-017	VDD	+3V3 ACRIX output
J2-018	VIN	+5V main power input
J2-019	I2C2_SDA	MCU I2C2 serial data, bidirectional, open-drain with pull-up
J2-020	VIN	+5V main power input
J2-021	I2C2_SCL	MCU I2C2 serial clock, open-drain with pull-up
J2-022	VIN	+5V main power input
J2-023	VDD	+3V3 ACRIX output
J2-024	VIN	+5V main power input
J2-025	SPI1_MISO	MCU SPI1 master input / slave output
J2-026	VDD	+3V3 ACRIX output
J2-027	N.C.	Not Connected
J2-028	#RESET	System reset, active low
J2-029	SDMMC1_D6	MCU SDMMC1 data bit 6
J2-030	GND	Ground (0V)
J2-031	SDMMC1_D7	MCU SDMMC1 data bit 7
J2-032	SDMMC1_D2	MCU SDMMC1 data bit 2
J2-033	SDMMC1_D4	MCU SDMMC1 data bit 4
J2-034	SDMMC1_D1	MCU SDMMC1 data bit 1
J2-035	GND	Ground (0V)
J2-036	GND	Ground (0V)
J2-037	SDMMC1_D5	MCU SDMMC1 data bit 5
J2-038	SDMMC1_D0	MCU SDMMC1 data bit 0
J2-039	SDMMC1_CMD	MCU SDMMC1 command / response line
J2-040	SDMMC1_D3	MCU SDMMC1 data bit 3
J2-041	GND	Ground (0V)
J2-042	GND	Ground (0V)
J2-043	GPIO_2	General-purpose input / output 2
J2-044	SDMMC1_CK	MCU SDMMC1 clock from host
J2-045	GPIO_3	General-purpose input / output 3

Pin	Signal	Description
J2-046	GPIO_13	General-purpose input / output 13
J2-047	GPIO_4	General-purpose input / output 4
J2-048	GPIO_9	General-purpose input / output 9
J2-049	GPIO_5	General-purpose input / output 5
J2-050	GPIO_8	General-purpose input / output 8
J2-051	UART8_RX	MCU UART8 receiver
J2-052	GND	Ground (0V)
J2-053	UART8_TX	MCU UART8 transmitter
J2-054	DBG_JTMS	MCU bidirectional data for SWD / TAP state machine control for JTAG
J2-055	GND	Ground (0V)
J2-056	GND	Ground (0V)
J2-057	CAN2_RX	MCU CAN2 receiver
J2-058	DBG_JTCK	MCU Serial Wire Debug / JTAG clock
J2-059	CAN2_TX	MCU CAN2 transmitter
J2-060	GND	Ground (0V)
J2-061	GND	Ground (0V)
J2-062	DBG_JTDO	MCU serial wire output trace / JTAG scan data out
J2-063	I2C4_SDA	MCU I2C4 serial data, bidirectional, open-drain with pull-up
J2-064	GND	Ground (0V)
J2-065	GND	Ground (0V)
J2-066	DBG_JTDI	MCU JTAG scan data input
J2-067	I2C4_SCL	MCU I2C4 serial clock, open-drain with pull-up
J2-068	GND	Ground (0V)
J2-069	GND	Ground (0V)
J2-070	DBG_NRST	MCU Serial Wire Debug / JTAG reset
J2-071	8SPI_P1_IO2	MCU OctoSPI P1 data bit 2
J2-072	8SPI_P1_IO1	MCU OctoSPI P1 data bit 1
J2-073	8SPI_P1_IO3	MCU OctoSPI P1 data bit 3
J2-074	8SPI_P1_IO0	MCU OctoSPI P1 data bit 0
J2-075	8SPI_P1_IO4	MCU OctoSPI P1 data bit 4
J2-076	8SPI_P1_DQS	MCU OctoSPI P1 data strobe, used in DTR mode for read data latching
J2-077	8SPI_P1_IO5	MCU OctoSPI P1 data bit 5
J2-078	8SPI_P1_NCS	MCU OctoSPI P1 chip select, active low
J2-079	8SPI_P1_IO6	MCU OctoSPI P1 data bit 6
J2-080	8SPI_P1_CLK	MCU OctoSPI P1 serial clock
J2-081	8SPI_P1_IO7	MCU OctoSPI P1 data bit 7
J2-082	GND	Ground (0V)
J2-083	N.C.	Not Connected
J2-084	USB_VBUS	+5V USB VBUS supply from host, or VBUS detect in device mode
J2-085	N.C.	Not Connected
J2-086	N.C.	Not Connected
J2-087	N.C.	Not Connected
J2-088	USB_CC1	USB Type-C configuration channel 1
J2-089	N.C.	Not Connected
J2-090	USB_CC2	USB Type-C configuration channel 2
J2-091	N.C.	Not Connected
J2-092	N.C.	Not Connected
J2-093	N.C.	Not Connected

Pin	Signal	Description
J2-094	N.C.	Not Connected
J2-095	N.C.	Not Connected
J2-096	N.C.	Not Connected
J2-097	N.C.	Not Connected
J2-098	N.C.	Not Connected
J2-099	GND	Ground (0V)
J2-100	GND	Ground (0V)

For more information regarding specific MCU or FPGA pins, please refer to the STM32H563ZIT6 or the ICE40UP5K datasheet.

7.4 Pinout diagram

The following pages show the connector pinout (J1 and J2) as a diagram. Signal names, power (VDD, VIN, GND), and function groups match the tables above.

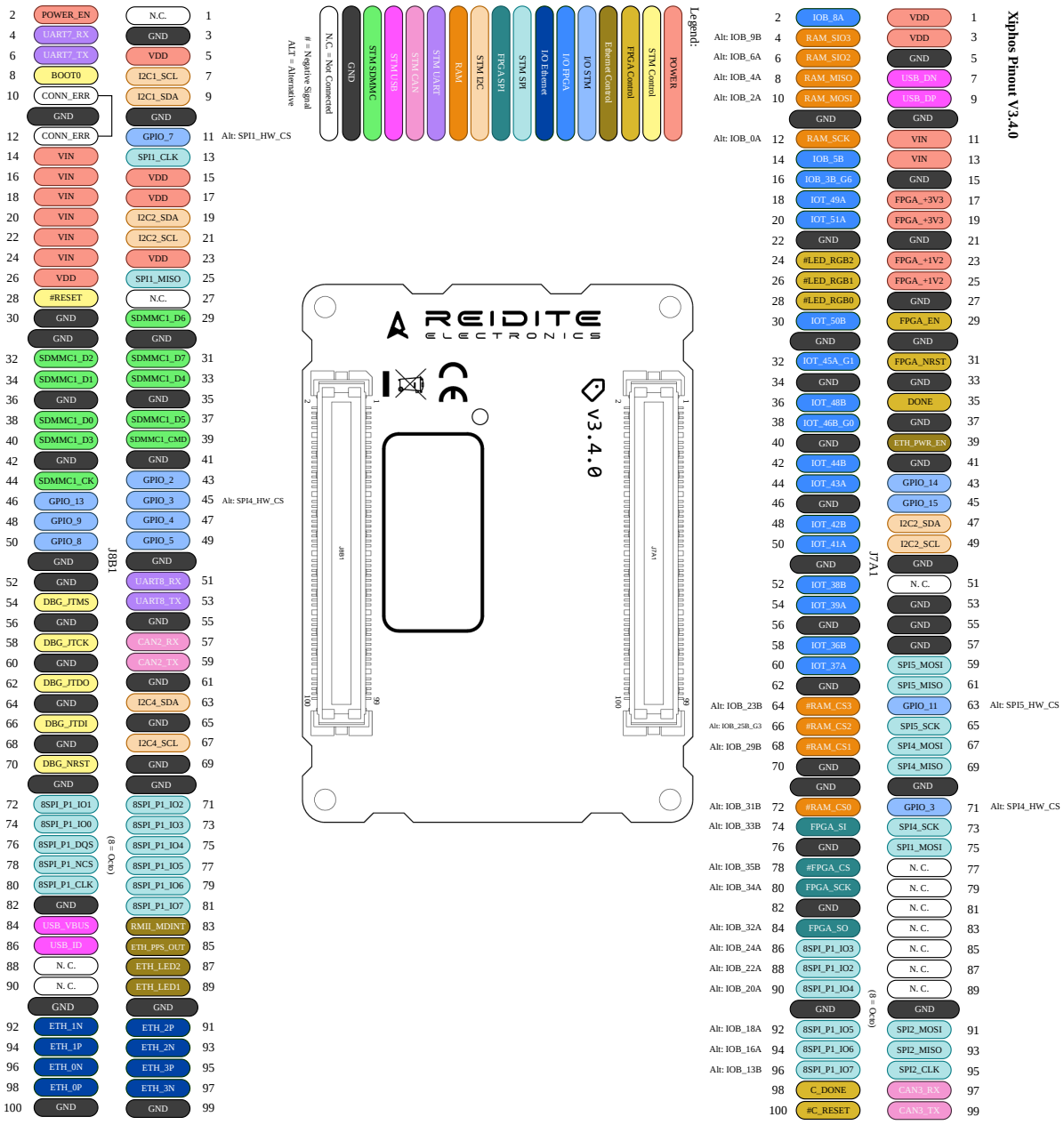

Figure 2: Pinout diagram with color-coded legend.

8 Power

ACRIX requires a single +5V supply with at least 600mA to work to its full potential. The TPS62132RGTR power regulator supplies the whole system. The FPGA module haS its own proprietary voltage regulators with enable pins controlled by the MCU. This helps with power efficiency when certain modules are not required. When power is applied, the MCU is the first to wake up. Then, based on the selection in the firmware package, the rest of the system is powered on. Please refer to our product page for our latest ACRIX software revision.

Note:

When powering off, please make sure all power has been disconnected from the module.

9 Troubleshooting

9.1 Module does not power up or show signs of life

- Check that the carrier supplies a stable 5V within the specified current capability and that polarity is correct.
- Verify that the module is fully seated on both connectors (J1 and J2).
- Inspect the connector area for bent pins, contamination, or damage.
- Confirm that the carrier board schematic matches the ACRIX pinout (power and ground pins in particular).

9.2 Debugger cannot connect (MCU)

- Ensure SWD/JTAG lines (and VDD, GND if required by the probe) are correctly routed from the carrier to the debug connector.
- Check that no other driver or application is holding the debug interface (close other IDEs or tools).
- Try a power cycle: remove power, wait a few seconds, then reapply and retry the connection.
- If the MCU was set to disable the debug port, use the bootloader (e.g. USB-DFU or UART) to recover or re-enable debug access as per the product documentation.

9.3 FPGA does not configure

- Verify JTAG connectivity and that the correct voltage levels are used for the FPGA I/O.
- If the bitstream is loaded by the MCU at boot, ensure the MCU firmware has loaded the correct image and that the storage (e.g. Flash) is accessible and intact.
- Check the Models Datasheet for the recommended configuration flow (JTAG vs MCU-loaded).

9.4 Other interfaces not working

- Confirm pin mapping and alternate function configuration in your firmware and carrier design.
- Review the electrical and operating conditions; ensure the module is within the specified temperature and supply limits.

9.5 Where to get help

For further support, contact REIDITE Industries with your module variant, carrier description, and a concise description of the symptom and steps already tried. Refer to the ordering section in the Family Datasheet for contact information.

10 Disclaimer

This document is released as version v1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Industries website and the ACRIX product page (downloads). For the latest specifications, always refer to the official datasheets and the REIDITE Industries website.