ACRIX Series

Datasheet

Open-frame (ACRIX-A1)

Phantom Forge® encapsulated (ACRIX-A2)

v1.0

June 29, 2026

Company: REIDITE Electronics
Document: ACRIX Datasheet
Status: Release 1.0 – Distribution

1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2025-02-02	Release 1.0 for distribution.
v1.1	2026-01-26	Pinout updated from official diagram; diagram embedded in Models datasheet; new Pinout reference document added.
v1.2	2026-01-19	

2 Hardware version guide

This documentation applies to ACRIX hardware version **1.1.0**. Ensure that your module and carrier design match this revision; for other hardware versions, contact REIDITE Electronics or refer to the ACRIX product page (downloads).

Contents

List of Figures

List of Tables

3 Overview

The ACRIX family is an industrial embedded computing platform aimed at control, communications, and signal processing applications in demanding environments. All modules have the same architecture with an STM32H5 microcontroller and a Lattice FPGA.

ACRIX is engineered as a robust industrial processor for harsh environments where reliability, deterministic behavior, and long-term availability are critical. The combination of a high-performance MCU with a low-power uFPGA provides both real-time control and adaptable hardware acceleration, enabling specialized interfaces, timing, and data-path customization without redesigning the core platform.

The family is designed to scale across performance and protection classes while maintaining a consistent software and electrical interface, simplifying reuse across product lines and reducing time to qualification.The MCU + FPGA approach provides an industrial alternative to Linux-based SoCs where deterministic timing and low complexity are required.

From a system integrator perspective, ACRIX balances deterministic control with hardware flexibility. The MCU handles real-time control loops, safety supervision, and communication stacks, while the FPGA provides timing-critical logic, protocol adaptation, and custom I/O. This division enables long-life, low-maintenance deployments without the overhead of a full Linux platform.

This document covers the family as a whole. Model-level specifications are provided in the *ACRIX Models Datasheet*.

4 System architecture

Every ACRIX module is built around the same core architecture: a high-performance microcontroller (MCU) for application and communication logic, and a small FPGA for timing-critical or protocol-specific hardware. This combination delivers deterministic real-time behaviour and hardware flexibility without the complexity of a Linux-based SoC, while acting as a suitable option when you need the power of iCE40 programmable logic without paying for integrated Ethernet, making ACRIX suitable for industrial automation, motor control, and connectivity-heavy edge applications.

4.1 Core elements

The main processor is the STM32H563ZIT6 from STMicroelectronics (), an ARM Cortex-M33 device running at up to 250 MHz with embedded Flash memory, hardware security features, and a broad set of integrated peripherals. The processor executes the main application stack, deterministic control functions, and system-level communication tasks through interfaces such as USB, CAN FD, UART, SPI, and I²C. The Lattice iCE40 UltraPlus FPGA (ICE40UP5K-SG48I) operates alongside the MCU and implements timing-critical or protocol-specific logic, including protocol adaptation, pulse generation, custom I/O expansion, and glue logic for legacy interfaces. Offloading these tasks to the FPGA allows the MCU to concentrate on application execution and system management, while the FPGA provides deterministic signal timing and precise control behavior.

- **Main MCU:** STM32H563ZIT6 (ARM Cortex-M33 up to 250 MHz).
- **FPGA:** Lattice iCE40 UltraPlus (ICE40UP5K-SG48I) for hardware acceleration and programmable I/O.

The STM32H563ZIT6 provides a robust real-time processing platform with deterministic interrupt handling, integrated performance optimization features, and a broad set of communication and peripheral interfaces. The FPGA acts as a flexible hardware fabric for I/O conditioning, state-machine implementation, and hardware handshake logic, enabling integration with legacy protocols and custom interfaces. This partitioning allows system designers to incorporate specialized functionality without the need for a separate external coprocessor while maintaining deterministic system behavior and implementation flexibility.

4.2 Common interfaces

All I/O is brought out to two 100-pin board-to-board connectors (Hirose FX11LA-100/10, J1 and J2), providing a consistent electrical and mechanical interface across the full ACRIX range. The available interfaces include general-purpose digital and analogue signals (SPI, I²C, UART, GPIO) and industrial connectivity (USB 2.0 OTG, CAN FD). Clock and reset signals are provided for synchronous system design. Interfaces are routed to the connector strips for clean mechanical integration and predictable signal mapping across variants, simplifying carrier-board design and allowing one carrier to support all ACRIX variants.

- SPI, I²C, UART, GPIO
- USB, CAN FD
- Industrial clock and reset

Designers should treat high-speed interfaces (USB, clock lines) as controlled-impedance signals and follow standard routing practices to minimize EMI and signal integrity issues. The shared pinout across all variants allows one carrier board to cover the full ACRIX range. For more information on our CarrierBoard, please refer to the product page.

5 Programming and debug

The MCU and FPGA are programmed using the official toolchains provided by their manufacturers.

5.1 MCU (STM32H563ZIT6)

- **Recommended interfaces:** SWD / JTAG (ST-LINK, J-Link, OpenOCD).
- **Bootloader options:** USB-DFU, UART, SPI, CAN (internal ROM bootloader).
- **Tooling:** STM32CubeIDE / STM32CubeMX, GCC ARM + GDB.

The MCU can be updated in the field without requiring JTAG access by using the built-in system bootloader. Firmware images are stored and executed from the integrated Flash memory available within the STM32H563ZIT6, eliminating the need for external memory devices.

Production firmware updates can be delivered through the bootloader, verified during the startup sequence, and managed using application-level validation mechanisms if required. This approach supports field maintenance and firmware deployment without opening the enclosure or exposing debug interfaces.

5.2 FPGA (ICE40UP5K-SG48I)

- **Development programming:** JTAG.
- **Production configuration:** bitstream loaded by the MCU at boot.
- **Toolchains:** Lattice iCEcube2 / Radiant, or open-source Yosys + nextpnr + IceStorm.

The FPGA can be configured persistently or loaded on each boot depending on the application workflow.

In typical deployments, the MCU verifies the FPGA bitstream integrity and loads it during boot, enabling secure and version-controlled hardware functions.

6 Phantom Forge® technology

REIDITE® Phantom Forge® is a packaging technology designed to improve environmental protection and thermal robustness while making the module difficult to access or tamper with. It is used on the ACRIX-A2 variant of ACRIX, which is intended for demanding industrial or outdoor-like environments where open-frame assemblies would be at risk from humidity, dust, vibration, or mechanical shock.

In the encapsulated version, the assembly is overmoulded with a protective layer that provides mechanical damping, moisture ingress protection, and improved resistance to ionising radiation and harsh electromagnetic fields. This enables operation in aggressive industrial atmospheres, wash-down scenarios, or outdoor installations where dust and water exposure are a concern. The technology supports an extended industrial temperature range and improves system stability in extreme industrial and field conditions. Variant selection depends on thermal conditions, vibration, and the required protection level for the application: open-frame variant (ACRIX-A1) for controlled or enclosed environments, and Phantom Forge® variant (ACRIX-A2) when environmental or mechanical stress justifies encapsulation.

- **ACRIX-A1:** unencapsulated (open-frame) version.
- **ACRIX-A2:** encapsulated version with Phantom Forge®.

Figure 1: Phantom Forge® encapsulated module (ACRIX-A2).

7 Key features

ACRIX combines an STM32H563ZIT6 ARM Cortex-M33 microcontroller with a Lattice iCE40 UltraPlus FPGA in a compact module architecture. This hybrid approach provides deterministic real-time operation and hardware flexibility without the complexity associated with Linux-based SoCs. The MCU executes the application stack, control functions, and communication interfaces, while the FPGA implements timing-critical logic, protocol adaptation, and custom I/O functionality. The FPGA extends the platform with adaptable hardware resources for state machines, signal conditioning, and interface customization, allowing support for legacy and application-specific protocols. The architecture enables designers to integrate specialized functionality without requiring additional coprocessors or dedicated hardware components. Optional secure boot and remote firmware update capabilities support in-field maintenance and reduced system downtime.

The family scales across packaging: open-frame variant (ACRIX-A1) for controlled environments, and Phantom Forge® encapsulated variant (ACRIX-A2) for harsh or outdoor-like conditions. All variants share the same pinout and software baseline, so one carrier board and one firmware baseline can cover the full range. The extended **industrial temperature range** (from **-40 °C** up to **85 °C**, **125 °C**, or **140 °C** depending on variant) and robust design for vibration, EMI, and harsh environments make ACRIX suitable for long-life industrial deployments. FreeRTOS and other RTOSes are commonly used; watchdog-based recovery and hardware-assisted diagnostics support resilient operation and faster fault isolation.

The following list summarises the main platform capabilities. Detailed MCU and FPGA specifications, pinout, and programming flows are provided in the models datasheet.

- Hybrid MCU + FPGA architecture.
- Secure boot and remote update support (optional).
- Scalability by packaging.
- Extended industrial temperature range (variant dependent).
- Deterministic timing and configurable data paths via FPGA logic.
- Robust design for vibration, EMI, and harsh environmental conditions.
- Consistent pinout and software baseline across the family.
- Hardware-assisted diagnostics for faster fault isolation.
- Supported RTOS: FreeRTOS.
- Watchdog-based recovery for resilient operation.
- **RoHS free** (all variants).

8 Target applications

- Industrial automation and process control
- Robotics and mechatronic systems
- Industrial communications and gateways
- Monitoring and data acquisition

The platform is well suited for edge systems requiring deterministic behavior, precise timing, and protocol adaptation, especially where mechanical and environmental robustness are key design constraints.

Typical deployments include factory controllers, transport monitoring units, energy management systems, and industrial gateways that require deterministic latency and long-life availability.

9 Comparison table

The following table provides a side-by-side comparison of the two ACRIX variants. It summarises the main differences in packaging (Phantom Forge®), and operating temperature so that the right model can be selected for each application.

Feature	ACRIX-A1	ACRIX-A2
Phantom Forge®	No	Yes
MCU (model)	STM32H563ZIT6	STM32H563ZIT6
MCU Flash (int.)	2 MB dual-bank Flash with ECC	2 MB dual-bank Flash with ECC
MCU SRAM (int.)	640 KB	640 KB
RAM (external)	None	None
Flash (external)	8 MB	8 MB
Lattice FPGA (model)	ICE40UP5K-SG48I	ICE40UP5K-SG48I
Ethernet	Not available in this board design	Not available in this board design
Min temperature	-40 °C	-40 °C
Max temperature	85 °C	125 °C

Table 1: Comparison of ACRIX-A1 and ACRIX-A2 variants, without and with Phantom Forge®encapsulation.

RoHS free: all ACRIX models.

10 Manufacturing and packaging

ACRIX is designed, developed, and assembled in Spain. Assembly is performed in qualified environments with controlled processes to minimize residues that could affect downstream industrial systems or sensitive applications. **All ACRIX modules are RoHS free.**

Process control includes ESD protection, particulate monitoring, and clean handling procedures. This reduces the risk of contamination in precision systems and ensures repeatable assembly quality over long production runs.

10.1 Packaging

Units are supplied in protective retail boxes for low-volume orders. For higher volumes, modules can be shipped in individual plastic trays to ensure handling protection and production-line compatibility.

Packaging is designed to prevent connector damage and maintain traceability throughout the logistics chain.

11 Quality and reliability

The ACRIX platform is intended for long-life industrial deployments where stability and predictable behavior are essential. The architecture favors component selection with extended availability and established supply chains, and the design prioritizes signal integrity, EMC resilience, and thermal margin.

Typical reliability-oriented characteristics include:

- Conservative clocking and power distribution for margin and longevity.
- Robust reset and watchdog strategies for fault recovery.
- EMC-conscious layout practices to reduce susceptibility and emissions.
- Support for environmental protection through Phantom Forge® encapsulation.

Qualification activities focus on repeatability, thermal cycling, and vibration stress. Designs are validated to sustain extended operation in industrial environments with minimal drift and consistent electrical behavior.

11.1 Certifications and protection

All ACRIX modules are RoHS free. The encapsulated variant meet **IP66** protection for dust and water ingress resistance.

12 Block diagram

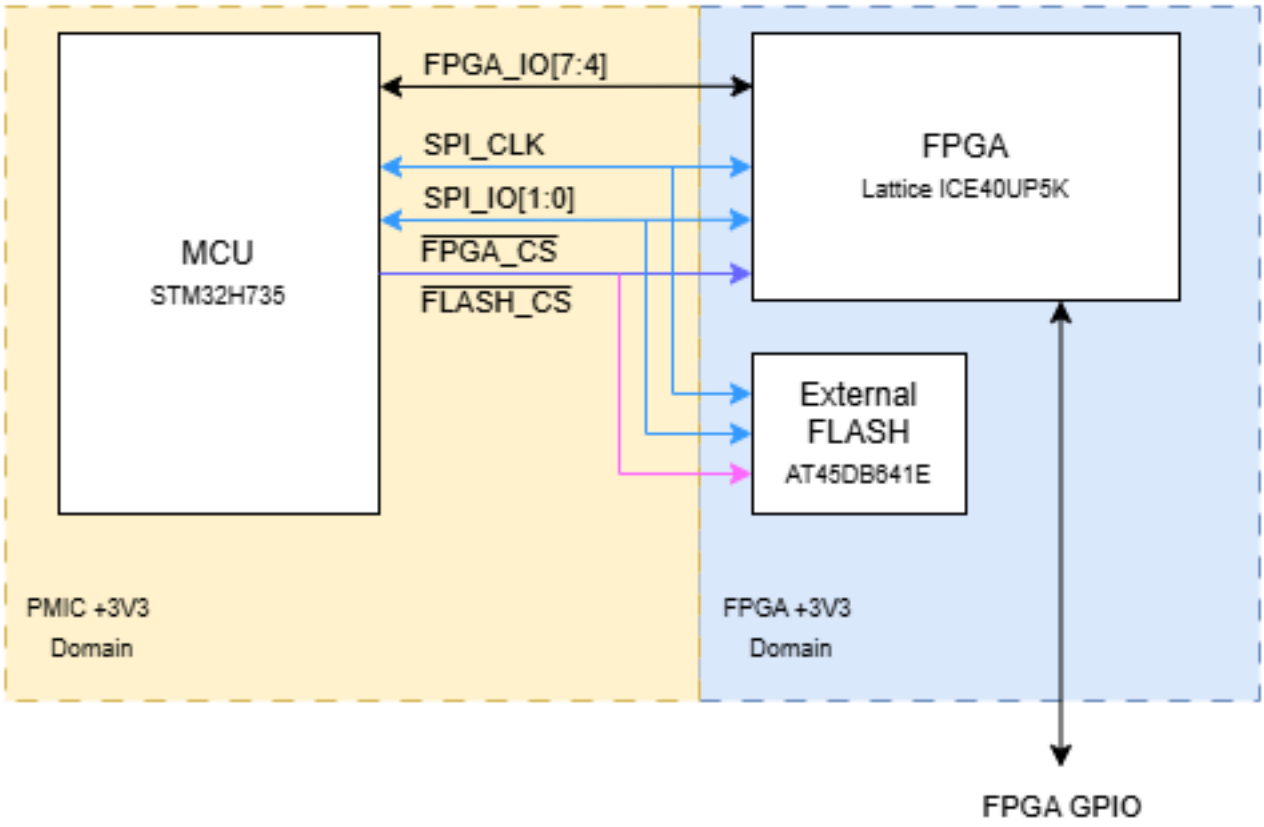

Figure 2: Block diagram of the ACRIX System for all variants.[1]

[1]FPGA +3V3 domain can be controlled by selected MCU pins. Please refer to ACRIX Datasheet for more information

13 Identification and ordering

Available variants are grouped by packaging and internal capabilities. Detailed specifications are provided in the Models Datasheet. For the latest document set and downloads, see the ACRIX product page (downloads).

Ordering should consider the required thermal envelope, and protection level.

ACRIX-A1	No Phantom Forge®
ACRIX-A2	With Phantom Forge®

14 Disclaimer

This document is released as version 1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Electronics website and the ACRIX product page (downloads). REIDITE Electronics reserves the right to make changes without notice.