



ACRIX Series

Models



Open-frame (ACRIX-A1)



Phantom Forge® encapsulated (ACRIX-A2)

v1.1

June 19, 2026

Company:	REIDITE Electronics
Document:	ACRIX Datasheet
Status:	Release 1.1 – Distribution



1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2025-02-02	Release 1.0 for distribution.
v1.1	2026-06-19	Pinout updated from official diagram; diagram embedded in Models datasheet; new Pinout reference document added.

2 Hardware version guide

This documentation applies to ACRIX hardware version **1.1.0**. Ensure that your module and carrier design match this revision; for other hardware versions, contact REIDITE Electronics or refer to the [ACRIX product page \(downloads\)](#).

Contents

1 Release evolution	2
2 Hardware version guide	3
3 Summary	6
4 MCU details (STM32H563ZIT6)	7
4.1 Summary of key parameters	7
5 FPGA details (ICE40UP5K-SG48I)	8
5.1 Summary of key parameters	8
6 Programming and debugging	9
6.1 MCU	9
6.2 FPGA	9
7 Connectors and carrier board	10
7.1 Integration notes	10
8 Comparison table	11
9 ACRIX-A1	12
9.1 Description	12
9.2 Notes	12
10 ACRIX-A2	13
10.1 Description	13
10.2 Notes	13
11 Operating conditions	14
11.1 General operating notes	14
11.2 Compliance and disposal	14
12 Electrical specifications	15
12.1 Input supply	15
12.2 Power states	15
13 Mechanical specifications	16
13.1 ACRIX-A1 (no Phantom Forge®)	16
13.2 ACRIX-A2 (with Phantom Forge®)	16
14 Disclaimer	17

List of Tables

1	Comparison of ACRIX-A1 and ACRIX-A2 variants, without and with Phantom Forge® encapsulation.	11
2	Input supply specifications.	15
3	Power states (typical current).	15

3 Summary

This document details the ACRIX-A1 and ACRIX-A2 variants of the ACRIX family. All models share the same base architecture: an STM32H5 microcontroller, and a Lattice iCE40 UltraPlus FPGA. The main differences between variants are packaging (open-frame versus Phantom Forge® encapsulation), and maximum operating temperature. This consistency allows a single software and hardware baseline to cover the full range, with drop-in upgrades when higher temperature or memory headroom is required.

The module exposes I/O through two 100-pin board-to-board connectors (Hirose FX11LA-100/10). These provide general-purpose signals and industrial interfaces, including SPI, I²C, UART, GPIO, USB, and CAN FD, as well as FPGA-programmable pins. The electrical mapping and pinout are consistent across all variants, so one carrier board design can support all variants.

ACRIX modules are assembled in qualified environments with controlled residue management to avoid contamination in industrial systems. **All ACRIX models are RoHS free.** The MCU + FPGA architecture delivers deterministic real-time control and hardware flexibility without the complexity of a Linux-based SoC, making it suitable for industrial automation, motor control, and connectivity-heavy edge applications.

4 MCU details (STM32H563ZIT6)

The industrial processor at the heart of every ACRIX module is the STM32H563ZIT6 from STMicroelectronics. This 32-bit ARM Cortex-M33 device combines deterministic real-time performance, integrated security features, and a large internal memory footprint, making it suitable for safety-conscious industrial applications without resorting to a Linux-based SoC.

The Cortex-M33 core runs at up to 250 MHz and includes an FPU, DSP instructions, an MPU, and Arm TrustZone support for hardware-assisted isolation between secure and non-secure firmware domains. The device integrates 2 MB of dual-bank internal Flash with ECC and 640 KB of internal SRAM, providing enough capacity for the application firmware, middleware, RTOS, and critical runtime data without requiring external RAM memories. An ART accelerator and instruction cache help reduce latency when executing from internal Flash, while the internal SRAM architecture supports predictable real-time operation for time-critical tasks.

On the connectivity side, the STM32H563ZIT6 provides USB 2.0 full-speed host/device capability, multiple UART/USART, SPI and I2C interfaces, two FDCAN controllers, SD/SDIO/MMC interfaces, advanced timers, high-speed 12-bit ADCs, DAC outputs, and a wide range of GPIOs. Although the STM32H563 family includes an Ethernet MAC peripheral, Ethernet is not used or exposed in this board design, so network connectivity is handled through the available non-Ethernet interfaces when required. Hardware security features such as TrustZone, secure/privileged memory regions, HASH acceleration, true random number generation, secure firmware installation support, secure firmware upgrade support, and authenticated debug help protect boot, update, and communication flows.

The module relies on the MCU internal Flash and SRAM as the primary execution and data memories, avoiding the complexity and validation burden of external RAM. If fitted, the external 8 MB Flash complements the MCU internal memory for firmware images, configuration storage, assets, or data logging, but it is not required as external volatile memory. The on-chip system bootloader supports in-field firmware updates without JTAG access through serial interfaces such as USART, I2C, SPI, CAN/FDCAN, or USB-DFU depending on the board routing and boot configuration, enabling maintenance and firmware recovery in deployed systems.

4.1 Summary of key parameters

- **CPU:** ARM Cortex-M33 up to 250 MHz.
- **Internal Flash:** 2 MB dual-bank Flash with ECC.
- **Internal SRAM:** 640 KB internal SRAM.
- **Cache / acceleration:** ART accelerator and instruction cache for reduced latency when executing from internal Flash.
- **Peripherals:** USB 2.0 full-speed host/device, FDCAN, UART/USART, SPI, I2C, SD/SDIO/MMC, ADCs, DACs, timers, GPIOs, crypto/security accelerators, HASH, and RNG.
- **RTOS support:** FreeRTOS and other real-time operating systems.

5 FPGA details (ICE40UP5K-SG48I)

The programmable logic on each ACRIX module is provided by a Lattice iCE40 UltraPlus device (part number ICE40UP5K-SG48I). This small-footprint FPGA sits between the MCU and the external I/O, enabling protocol adaptation, deterministic timing generation, and custom glue logic without adding a separate discrete ASIC or a more complex SoC. The microcontroller and FPGA work together to form a flexible compute pair: the MCU runs the application and communication stack, while the FPGA handles time-critical or protocol-specific tasks with predictable latency.

The iCE40 UltraPlus offers approximately 5280 4-input LUTs with associated flip-flops and about 120 kbit of embedded block RAM. In ACRIX, the FPGA is typically used at clock rates below 50 MHz, which keeps power and signal-integrity margins comfortable while still supporting real-time interfaces such as custom serial protocols, pulse generation, or multiplexed I/O expansion. The core voltage is nominally 1.2 V; the exact number of user I/O pins available depends on the package and the integration with the MCU and connectors.

Typical ACRIX usage includes protocol adaptation (e.g. translating between legacy industrial buses and the MCU), deterministic timing generation for actuators or sensors, and custom I/O logic where sub-microsecond response is required. By offloading these functions to the FPGA, the MCU is freed to handle application logic, networking, and storage, while the FPGA ensures deterministic signal timing and precise control loops. The bitstream can be loaded by the MCU at boot or from external storage, allowing field updates of FPGA behaviour without physical access to the board.

5.1 Summary of key parameters

- **Family:** Lattice iCE40 UltraPlus.
- **Logic capacity:** ~5280 LUTs (4-LUT + FF).
- **Internal RAM:** ~120 kbit SRAM.
- **I/O count:** ~39 programmable pins (package dependent).
- **Typical frequency:** < 50 MHz (design dependent).
- **Core voltage:** ~1.2 V.

6 Programming and debugging

ACRIX supports both development-time debugging and production or in-field firmware updates. The MCU and FPGA can be programmed and debugged via standard interfaces; the choice of method depends on the development phase and whether physical access to the board is available.

6.1 MCU

The STM32H563ZIT6 is programmed and debugged via SWD or JTAG using tools such as ST-LINK, J-Link, or OpenOCD. Development is typically done with STM32CubeIDE or STM32CubeMX for project setup, and with GCC ARM and GDB for building and debugging. The MCU incorporates an on-chip system bootloader in ROM that supports several serial entry points for firmware updates, including USB-DFU, USART, I2C, SPI, and CAN/FDCAN, depending on the board routing and boot configuration. Thus, in production or in the field, the application can be updated without JTAG access: the device is placed in bootloader mode, for example via the BOOT0 pin, a dedicated GPIO-controlled sequence, or an application-level jump to the system memory bootloader, and the new image is delivered over USB, UART, CAN/FDCAN, or another supported and routed interface. This reduces dependency on debug connectors and simplifies deployment, recovery, and maintenance.

- **Debug/programming:** SWD / JTAG using ST-LINK, J-Link, OpenOCD, or compatible probes.
- **Bootloader:** USB-DFU, USART, I2C, SPI, and CAN/FDCAN
- **Tooling:** STM32CubeIDE / STM32CubeMX, GCC ARM + GDB.

6.2 FPGA

During development, the Lattice iCE40 FPGA is typically programmed via JTAG using Lattice iCEcube2 or Radiant, or with the open-source toolchain (Yosys, nextpnr, IceStorm). In production and in the field, the FPGA bitstream is often stored in external Flash or in the MCU filesystem and loaded by the MCU at boot. The MCU can verify the bitstream (e.g. with a checksum or signature) before configuring the FPGA, so that field updates of FPGA functionality are possible without physical access to the board. Care must be taken when configuring the FPGA. It is recommended to document whether the configuration is persistent in the FPGA or reloaded on each boot in your system integration flow, as this affects startup time and update procedures.

- **Development programming:** JTAG.
- **Production configuration:** bitstream loaded by the MCU at boot.
- **Toolchains:** Lattice iCEcube2 / Radiant, or open-source Yosys + nextpnr + IceStorm.

7 Connectors and carrier board

All I/O between the ACRIX module and the carrier board is brought out through two 100-pin board-to-board connectors, **Hirose FX11LA-100/10**, designated J1 and J2. These connectors provide a dense, reliable interface for power, ground, and the full set of digital and analogue signals (SPI, I²C, UART, GPIO, USB, CAN FD, and FPGA I/O). Carrier-board designers must use the vendor-recommended mating connector and footprint to guarantee mechanical fit, electrical contact, and long-term reliability. For more information on our CarrierBoard, please refer to the [product page](#).

Connector placement, orientation, and stack height are defined in the mechanical documentation. Validate your carrier layout against those drawings to ensure clearance, tolerance compliance, and correct mating sequence during assembly. Incorrect stack height or misalignment can lead to intermittent contacts or damage to the connectors.

JTAG and SWD pins are available on the connector for debug and factory programming. Many MCU and FPGA pins are multiplexed and require firmware or bitstream configuration to match the intended function; consult the pinout and application notes when assigning signals. Unless explicitly stated in the pinout, pins are not 5 V tolerant and must not be driven above the MCU or FPGA I/O voltage. For signal integrity, route USB and clock signals with controlled impedance and minimize crosstalk with other high-speed or sensitive lines.

Reidite Industries provides

7.1 Integration notes

- JTAG/SWD pins are provided for debug and factory programming.
- Some pins are multiplexed and require firmware configuration.
- Pins are not 5 V tolerant unless explicitly stated.
- Route USB and clock signals with controlled impedance.

8 Comparison table

The following table provides a side-by-side comparison of the two ACRIX variants. It summarises the main differences in packaging (Phantom Forge®), and operating temperature so that the right model can be selected for each application.

Feature	ACRIX-A1	ACRIX-A2
Phantom Forge®	No	Yes
MCU (model)	STM32H563ZIT6	STM32H563ZIT6
MCU Flash (int.)	2 MB dual-bank Flash with ECC	2 MB dual-bank Flash with ECC
MCU SRAM (int.)	640 KB	640 KB
RAM (external)	None	None
Flash (external)	8 MB	8 MB
Lattice FPGA (model)	ICE40UP5K-SG48I	ICE40UP5K-SG48I
Ethernet	Not available in this board design	Not available in this board design
Min temperature	-40 °C	-40 °C
Max temperature	85 °C	125 °C

Table 1: Comparison of ACRIX-A1 and ACRIX-A2 variants, without and with Phantom Forge® encapsulation.

RoHS free: all ACRIX models.

9 ACRIX-A1

9.1 Description

The ACRIX-A1 is the **base variant** of the family: a compact module combining the **STM32H563ZIT6** MCU and the **Lattice iCE40 UltraPlus** FPGA without Phantom Forge® encapsulation. It is designed for integration into **controlled environments** or into carrier boards and enclosures that already provide mechanical support, thermal management, and environmental protection. The ACRIX-A1 offers the same processing and connectivity capabilities as the rest of the family (USB, CAN FD, programmable FPGA I/O) with a lower maximum operating temperature, making it suitable for cost-sensitive or space-constrained applications where moderate thermal and memory requirements are sufficient.

9.2 Notes

ACRIX-A1 targets controlled environments where compact size and baseline functionality are prioritised. It is suitable for applications with moderate thermal requirements, such as indoor industrial equipment, lab instruments, or embedded systems inside a protected enclosure. For harsher conditions or higher memory needs, consider the ACRIX-A2 (encapsulated), or XIPHOS family (PSRAM, Ethernet).

10 ACRIX-A2

10.1 Description

The ACRIX-A2 is the base variant with **Phantom Forge® encapsulation**. It shares the same MCU, and FPGA, but is protected by the Phantom Forge® overmould, which improves resistance to humidity, dust, and mechanical stress and provides **IP66** ingress protection. The maximum operating temperature is **140 °C**, making the ACRIX-A2 suitable for **demanding industrial environments** where open-frame boards would be at risk: high-vibration machinery, wash-down or outdoor-like conditions, or applications where long-term reliability under thermal and environmental stress is critical.

10.2 Notes

ACRIX-A2 combines Phantom Forge® encapsulation with high-temperature capability for robust deployments in harsh industrial environments. It is the right choice when environmental or mechanical conditions rule out open-frame variants but when the application does not require the extra 32 MB PSRAM of the XIPHOS family. For maximum memory and robustness, and overall improved performance, the XIPHOS-X4 variant of the XIPHOS family offers both encapsulation and external PSRAM.

11 Operating conditions

ACRIX modules are specified for industrial environments where thermal, mechanical, and electrical stress are higher than in typical commercial applications. All variants support an operating temperature range starting at **-40 °C**; the upper limit depends on the variant (**85 °C** for ACRIX-A1, and **140 °C** for ACRIX-A2). These limits assume that the module is used within the specified supply and interface conditions and that adequate cooling or thermal coupling is provided when the system runs at high load for extended periods.

In applications with high ambient temperature or limited airflow, thermal design of the carrier and enclosure is critical. The open-frame variant (ACRIX-A1) rely on the end product to provide mechanical protection and, where needed, environmental sealing; the Phantom Forge® variant (ACRIX-A2) offer improved resistance to humidity and contamination and are better suited to harsh or outdoor-like conditions. Condensation should be avoided on unencapsulated assemblies; in high-humidity or wash-down scenarios, the encapsulated version is recommended.

EMC performance depends on the full system: PCB layout, enclosure, cables, and software. When integrating high-speed I/O (USB, etc.), follow controlled-impedance routing and grounding practices and validate emissions and immunity at the system level.

11.1 General operating notes

- Ensure adequate airflow or thermal coupling for sustained high load.
- Avoid condensation; use Phantom Forge® variants in harsh humidity.
- Validate EMC behavior at system level when integrating high-speed I/O.

11.2 Compliance and disposal

All ACRIX models are RoHS free. The encapsulated variant (ACRIX-A2) is rated to **IP66** for ingress protection, making them suitable for demanding industrial or outdoor installations where dust and water exposure are a concern.

Do not dispose of this equipment with household waste. Electronic assemblies must be handled through controlled waste management and delivered to an appropriate electronics recycling container or authorized collection point.

Environmental limits (temperature, humidity, mechanical shock) should be validated at the system level, including enclosure thermal behavior, airflow, and connector selection.

12 Electrical specifications

ACRIX modules are designed to be powered from a single **5 V** supply provided by the carrier board through the board-to-board connectors. All internal regulation (e.g. for the MCU and FPGA core voltages) is handled on-module, so the system integrator only needs to provide a stable 5 V rail within the specified current range. This simplifies carrier design and avoids multiple external regulators.

12.1 Input supply

The module accepts a nominal input voltage of 5 V. The minimum current figure corresponds to a lightly loaded state (e.g. MCU in low-power mode with the FPGA unconfigured or idle); the maximum current covers full operation with MCU and FPGA active, USB in use, and typical I/O switching. The exact consumption depends on clock rates, peripheral usage, and FPGA bitstream. For margin in the end application, plan for the maximum current and ensure the 5 V source can sustain it without excessive droop. The main electrical limits are given in Table 2.

Parameter	Value
Input voltage	5 V
Minimum current	19 mA
Maximum current	280 mA

Table 2: Input supply specifications.

12.2 Power states

Different power states (e.g. standby, run with MCU only, run with MCU and FPGA) are available to balance performance and consumption. Exact current and wake-up behaviour for each state are documented in the product-specific datasheet or application notes. Power profiling should be performed in the target system to account for peripheral load, external transceivers, and connector configuration. Table 3 summarises the main power states.

State	Current
Standby	TBD
Run (MCU)	TBD
Run (MCU + FPGA)	TBD

Table 3: Power states (typical current).

13 Mechanical specifications

The mechanical form factor of ACRIX is common to all variants: a compact module with a nominal PCB size of 55 mm × 40 mm and two connector strips along one or two edges for mating with the carrier board. Four M2.5 screw holes are placed at each corner for mechanical fastening. Dimensions, tolerances, keepout zones, and connector positions are detailed in the Mechanical Datasheet and the [ACRIX product page \(downloads\)](#).

13.1 ACRIX-A1 (no Phantom Forge®)

The ACRIX-A1 variant is supplied as an open-frame PCB assembly: the MCU, FPGA, memories, and passives are mounted on the board, but there is no overmould or enclosure on the module itself. This version is intended for integration into protected enclosures or carrier boards that provide mechanical support, thermal management, and environmental shielding. It is suited to cost-sensitive or space-constrained applications where the end product already provides the required protection.

- PCB dimensions: 55 mm × 40 mm
- Maximum component height: see mechanical datasheet
- Connectors: two strips for power, ground, and signals (SPI, I²C, USB, CAN FD, etc.)

13.2 ACRIX-A2 (with Phantom Forge®)

The ACRIX-A2 variant is encapsulated using Phantom Forge® technology, which adds a protective layer over the assembly, improves resistance to humidity and contamination, and can enhance mechanical damping in high-vibration environments. The encapsulated version is recommended for harsh industrial or outdoor-like installations where open-frame boards would be at risk. The external dimensions remain 55 mm × 40 mm at the PCB level; the encapsulant may add a small amount to the overall stack height. Thermal anchor points and protection ratings are given in the mechanical document.

- Encapsulated dimensions: 57,6mm × 42,6mm
- Thermal anchor points: see mechanical datasheet
- Connectors: two strips for power, ground, and signals (SPI, I²C, USB, CAN FD, etc.)
- Protection rating: IP66 for encapsulated variants

When using a Phantom Forge® variant, allow adequate thermal coupling to the carrier or chassis to maximize heat transfer under high-temperature conditions and follow the mounting and keeping guidelines in the mechanical datasheet.

14 Disclaimer

This document is released as version 1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Electronics website and the [ACRIX product page \(downloads\)](#). REIDITE Electronics reserves the right to make changes without notice.