



# Carrier Board DEV-ETH

Datasheet

v1.0

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## 1 Release evolution

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The following table lists document releases and their dates.

<b>Version</b>	<b>Date</b>	<b>Changes</b>
v1.0	2026-05-28	Release 1.0 for distribution.

## 2 Hardware version guide

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This documentation applies to Carrier Board DEV-ETH hardware version **1.1.0**. Ensure that your module or carrier design match this revision; for other hardware versions, contact REIDITE Industries or refer to the [Carrier Board DEV-ETH product page \(downloads\)](#).

### 3 Introduction

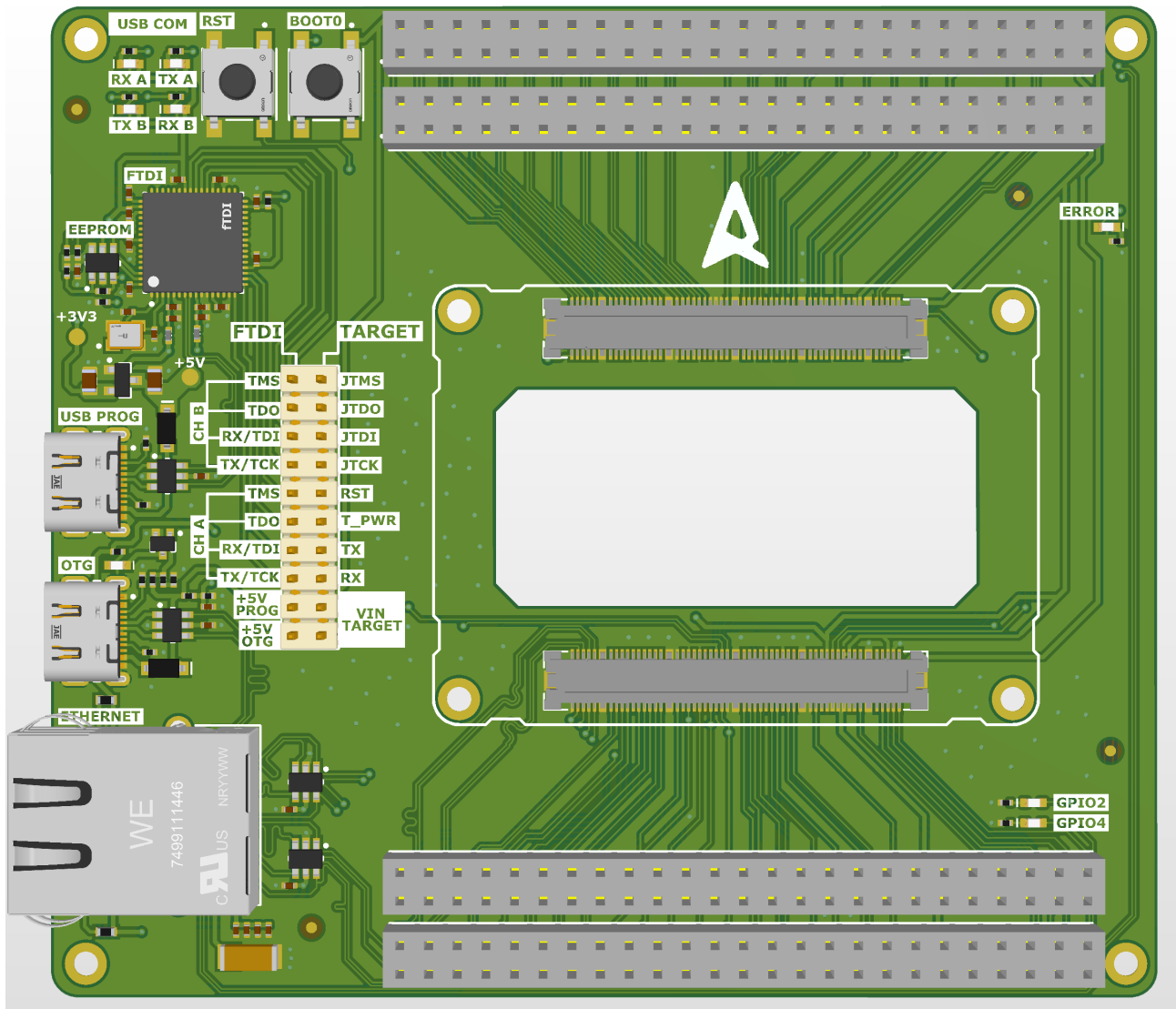


Figure 1: Render of the Carrier Board DEV-ETH 1.1.0

The Carrier Board DEV-ETH from REIDITE Industries is a motherboard-like development platform designed for interfacing, programming, testing, and debugging System-on-Modules (SoMs), such as the XIPHOS Module. This system reduces the effort required to design a proprietary carrier solution by providing a simplified, portable, and easy-to-use interface with USB-C, Ethernet connectivity. Additionally, the development board provides access to all 200 pins, enabling users to evaluate, monitor, and debug each signal individually.

## 4 Features

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- Ethernet RJ45 MagJack connector
- USB 2.0 connectivity with OTG support through a USB-C connector
- Dedicated USB-C connector for FTDI programming and debugging
- FTDI interface with two independent channels for programming and communication
- Real-time debugging support
- Communication status LEDs
- SoM orientation error indicator LED
- Reset and Boot push buttons
- 2 kV ESD protection

### 4.1 Power

The Carrier Board DEV-ETH can be powered through its USB-C interfaces at +5 V. The required supply current depends on the connected SoM, while the carrier board is rated to support up to 1 A. Power routing to the target SoM can be configured using the dedicated jumpers. Electrostatic discharge (ESD) protection is implemented on all connectors. Proper ESD-safe handling precautions should still be observed when operating, connecting, or handling the device.

**Note:**

Before disconnecting the module, ensure that all power has been cut-off from the carrier board.

### 4.2 Ethernet

The board integrates an RJ45 Ethernet connector with built-in magnetics. Additional ESD protection and decoupling components are included to improve board-level protection and signal integrity. The interface supports 10/100 Mb/s data transfer rates.

### 4.3 USB 2.0

The Carrier Board DEV-ETH includes two USB-C connectors. One connector is dedicated to the FTDI interface for programming, debugging, and communication, while the second connector provides USB 2.0 OTG connectivity to the target SoM.

Both USB-C connectors can be used to power the target SoM through the dedicated power-selection jumpers. However, powering the target SoM from both USB-C connectors at the same time is not recommended. Only one USB-C power source should be selected at a time to avoid unintended power-path conflicts.

### 4.4 GPIOs

Four 50-pin, dual-row female headers are provided for interfacing the 200+ pins of the SoM. This allows the user to test and debug every pin and to connect external modules if needed.

**Note:**

Not all GPIO pins are 5 V tolerant. For additional information regarding GPIO configuration and electrical characteristics, refer to the [documentation page](#).

## 4.5 Jumpers

The Carrier Board DEV-ETH includes a dedicated A 20-pin, dual-row male header for configuring power routing and interface selection. These jumpers allow the user to select the USB-C power source for the target SoM and configure the desired operating mode according to the application requirements. It also provides access to both FTDI channels for programming and communication. Both channels support JTAG, SWD, and UART protocols.

Pin	Function
TMS/CS (CH_B)	FTDI Pin; Test Mode Select; Output Signal Select; Channel B
TDO/DI (CH_B)	FTDI Pin; Test Data Output; Serial Data Input; Channel B
RX/TDI/DO (CH_B)	FTDI Pin; Receiver Input; Test Data Input; Serial Data Output; Channel B
TX/TCK/SK (CH_B)	FTDI Pin; Transmitter output; Clock signal output; Serial Clock; Channel B
TMS/CS (CH_A)	FTDI Pin; Test Mode Select; Serial Chip Select; Channel A
TDO/DI (CH_A)	FTDI Pin; Test Data Output; Serial Data Input; Channel A
RX/TDI/DO (CH_A)	FTDI Pin; Receiver Input; Test Data Input; Serial Data Output; Channel A
TX/TCK/SK (CH_A)	FTDI Pin; Transmitter Output; Test Interface Clock; Serial Clock; Channel A
+5V_PROG	+5V Power input from USB-C PROG connector.
+5V_OTG	+5V Power input from USB-C OTG connector.
DBG_JTMS_SWDI	SWDIO TARGET Pin; Test Mode Select
DBG_JTDO_SWO	SWDIO TARGET Pin; Test Data output
DBG_JTDI	SWDIO TARGET Pin; Test Data Input
DBG_JTCK_SWCL	SWDIO TARGET Pin; Test interface clock
#RESET	System reset. Active low.
VDD	This power source comes from selected SoMs (like XIPHOS). It is at least +3.3 volts. It proves if the target is receiving power and outputting correctly. It can also serve for powering external devices.
UART_TX	TARGET Pin; Transmitter output
UART_RX	TARGET Pin; Receiver input
+5V_PROG	Power source for SoM, coming from the FTDI USB-C connector.
+5V_OTG	Power source for SoM, coming from the USB-C OTG connector.

**Note:**

For additional information about the FT2232HQ device, channel configuration, and drivers, refer to the [FTDI product page](#).

## 4.6 LEDs

### 4.6.1 Error LED

This LED is activated when the SoM is incorrectly oriented after being installed on the carrier board. The SoM board is correctly connected when the two Reidite Logos (the one in the carrier and the one in the SoM) are aligned.

### 4.6.2 GPIO LEDs

Two GPIO LEDs are available on the board for user-defined or multipurpose configuration. GPIO LED 2 is red, and GPIO LED 4 is green.

### 4.6.3 USB OTG LED

This LED is activated when USB OTG communication is established with the SoM. It also functions as a power indicator when the board is powered through the USB-C OTG connector.

### 4.6.4 FTDI LEDs

Four blue LEDs indicate the communication direction, TX and RX, for both FTDI channels A and B.

## 5 Mechanical Drawings

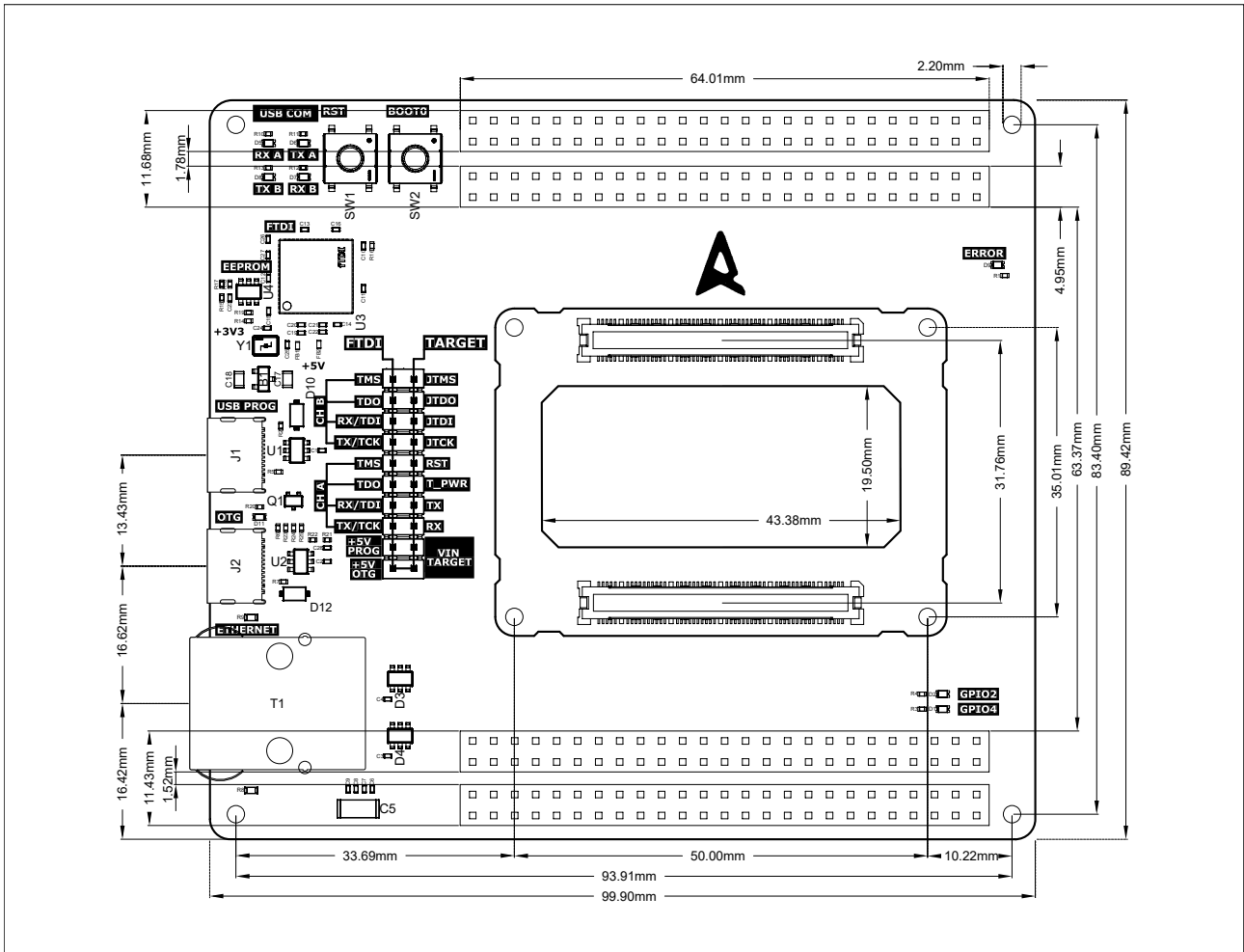


Figure 2: Mechanical drawings of the Carrier Board DEV-ETH Board.

## 6 Pinout diagram

The following figure shows the connector pinout of J6, J7, J3 and J4 of the carrierboard with its respective FX11 connector. All GND pins are shown in black.

Carrierboard Pinout V1.1.0

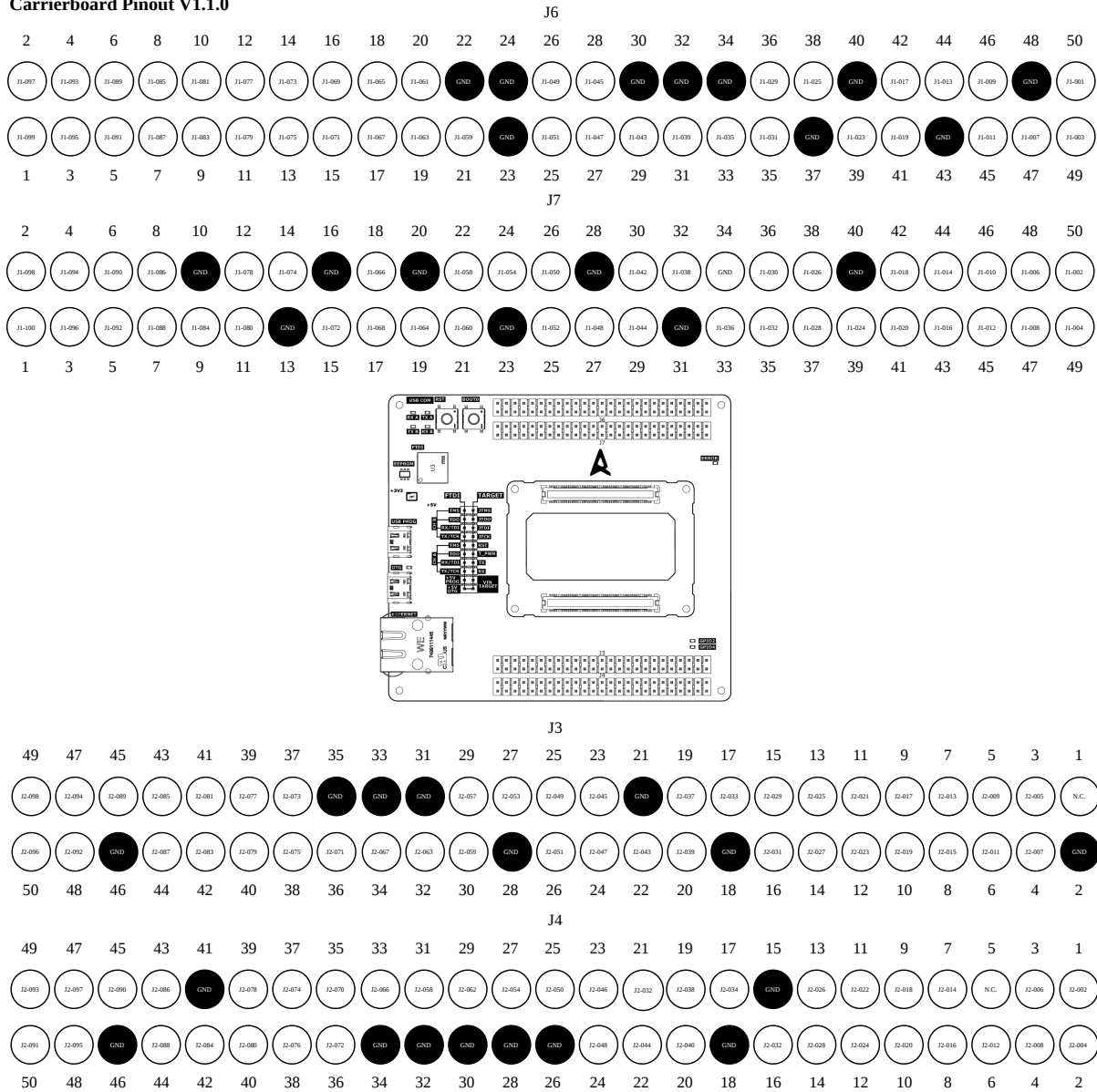


Figure 3: Carrierboard Pinout diagram

**Note:**

N.C. = Not Connected