REIDITE INDUSTRIES

XIPHOS Series

Datasheet

Open-frame (XIPHOS-X1 / XIPHOS-X2)

Phantom Forge® encapsulated (XIPHOS-X3 / XIPHOS-X4)

v1.0

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1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2026-05-22	Release 1.0 for distribution.

2 Hardware version guide

This documentation applies to XIPHOS hardware version **3.4.0**. Ensure that your module and carrier design match this revision; for other hardware versions, contact REIDITE Industries or refer to the XIPHOS product page (downloads).

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3 Introduction

Open-frame (XIPHOS-X1 / XIPHOS-X2)

Phantom Forge® encapsulated (XIPHOS-X3 / XIPHOS-X4)

The XIPHOS X1/X2/X3/X4 are a series of System-On-Module (SoM) devices aimed at control, communications, and signal processing applications for demanding environments. Thanks to it's patented technology Phantom Forge®the system can sustain up to 140ºC of temperature and meets IP66 rating for particle and water resistance. This SoM embeds a powerful MCU coupled with an FPGA for industrial scenarios where power efficency, flexibility and reliability are key aspects.

The family is designed to scale across performance and protection classes while maintaining a consistent software and electrical interface, simplifying reuse across product lines and reducing time to qualification.

The XIPHOS module has CE Marking homologation and EMC certification.

3.1 Key features

- Hybrid MCU STM32H735xG + ICE40UP5K architecture.
- Industrial Ethernet with integrated PHY.
- Secure boot and remote update support (optional).
- Options for 0MB (XIPHOS X1-X3), 32MB of PSRAM (XIPHOS X2-X4).
- Extended industrial temperature range (variant dependent).
- Deterministic timing and configurable data paths via FPGA logic.
- Consistent pinout and software baseline across the family.
- Supported RTOS: FreeRTOS.
- Rich MCU GPIO:
  - 11 proprietary GPIO pins
  - 29 x FPGA GPIO Pins
  - 1 x RMII Ethernet up to 100MB/s
  - 2 x UART
  - 2 x CAN
  - 4 x I²C

  - 5 x SPI
  - 1 x OctoSPI
  - 1 x USB 2.0 (High Speed)
  - 1 x SDMMC
- Small footprint 55 mm × 40 mm (without encapsulation); 57,6mm × 42,6mm (with encapsulation)
- 4 x M2.2 mounting holes
- **RoHS free** (all variants).

4 Interfaces

4.1 Power Monitoring

The SoM integrates an INA226AQ chip for real-time measurmente of current, voltage and power consumption. This chip is directly communicated to the main MCU STM32H735 through an I²C interface.

- Bus voltage monitoring
- Current sensing
- Power calculation
- Programmable alert functionality
- High-side current measurement

4.2 Ethernet

The board integrates an VSC8531XMW-02 Gigabit Ethernet PHY chip connected to the STM32H735IGT6 microcontroller through an RMII interface. The Ethernet PHY supports:

- 10BASE-T
- 100BASE-TX

The differential MDI pairs are routed to the module connector for connection to external Ethernet magnetics and RJ45 circuitry implemented on the carrier board.

Signal Name	Description
ETH_0P/ETH_0N	MDI differential pair 0
ETH_1P/ETH_1N	MDI differential pair 1
ETH_2P/ETH_2N	MDI differential pair 2
ETH_3P/ETH_3N	MDI differential pair 3

Table 1: Exposed Ethernet Signals

4.2.1 Features

- IEEE 802.3 compliant PHY
- RMII MAC-to-PHY interface
- Automatic MDI/MDIX detection

4.3 USB 2.0

Integration of USB 2.0 interface through the USB controller of the STM32H735IGT6 microcontroller. The USB interface signals are routed to the module connector for implementation on an external carrier board.

4.3.1 Features

- USB 2.0 compliant interface
- USB OTG support
- Integrated USB controller in STM32H735IGT6

Signal Name	Description
USB_VBUS	USB bus voltage detection
USB_ID	USB OTG identification signal
USB_DP	USB differential data positive
USB_DN	USB differential data negative

Table 2: Exposed USB Signals

4.4 XIPHOS GPIO Interface

The board exposes 11 general-purpose input/output (GPIO) signals provided by the STM32H735IGT microcontroller to the module connector. GPIO signals operate at 3.3 V logic levels and are not 5 V tolerant unless explicitly stated in the STM32H735IGT datasheet. Each GPIO can be configured by firmware as:

- Digital input
- Digital output
- External interrupt source
- Alternate peripheral function

4.4.1 Features:

- 3.3 V CMOS logic levels
- Firmware-configurable direction and function
- Internal pull-up and pull-down resistor configuration
- External interrupt capability on supported pins
- Alternate peripheral functions depending on pin assignment

4.4.2 FPGA GPIO Interface

The board exposes 29 user-programmable FPGA I/O signals from the Lattice iCE40 FPGA to the module connector. These signals may be configured through FPGA configuration to implement custom digital interfaces and logic functions.

4.4.3 Features:

- User-programmable FPGA I/O
- Direct FPGA fabric connectivity
- Custom digital interface implementation capability
- FPGA-defined signal functionality

4.5 CAN

The device supports CAN signal routing from the STM32H735IGT6 microcontroller to the module connector. An external CAN transceiver on the carrier board is required to interface these signals with a physical CAN bus.

Signal Name	Description
CAN2_TX	CAN2 transmit signal from MCU
CAN2_RX	CAN2 receive signal to MCU
CAN3_TX	CAN3 transmit signal from MCU
CAN3_RX	CAN3 receive signal to MCU

Table 3: Exposed CAN Signals

Features:

- STM32 integrated FDCAN controller
- Classic CAN support
- CAN FD support, depending on firmware configuration
- External CAN transceiver required on carrier board

4.6 SPI

The board exposes multiple SPI interfaces for high-speed synchronous serial communication.

Interface	Function
SPI1	External Interface
SPI2	External Interface
SPI3	External Interface
SPI4	External Interface

Table 4: Exposed SPI Signals

The SPI interfaces operate at 3.3V logic levels and may be used for communication with external peripherals such as:

- Sensors
- ADC/DAC devices
- Displays
- External controllers
- Memory devices

4.7 FPGA SPI

When the module starts for the first time, the FPGA does not contain any preconfigured firmware. Therefore, the MCU is responsible for uploading the firmware by programming the external flash memory. Once the firmware has been uploaded (and after a hard reset), the FPGA loads and executes the code stored in the flash through the shared SPI communication bus.

This SPI bus is shared between the MCU, the FPGA, and the external flash memory. Although the four communication lines are routed to the FX11 connectors, it is recommended not to use this bus for purposes other than its intended operation.

4.8 I²C

The board exposes multiple I²C interfaces for peripheral communication and system monitoring.

Interface	Function
I²C1	External peripheral expansion
I²C2	External peripheral expansion
I²C4	Internal monitoring and FPGA communication

Table 5: Exposed I²C Signals

I²C4 is used internally for communication between the FPGA subsystem and the INA226 power monitor. All I²C interfaces operate at 3.3V logic levels. External pull-up resistors may be required depending on bus topology and connected peripherals.

5 Electrical & Mechanical

5.1 Electrical specification

This section shows the absolute maximum limits of the system. Values exceeding those in Table 6 may cause permanent damage to the device.

Symbol	Parameter	Minumum	Maximum	Unit
V_{in}	Input Voltage	-0.3	20	V
V_{GPIO_REF}	GPIO Voltage	-0.35	3.6	V
V_{GPIO}	GPIO Input Voltage	-0.35	3.76	V

Table 6: Absolute Maximum Limits

Symbol	Parameter	Conditions	STM32H735	iCE40UP5K	Unit
V_{DD}	Core / I/O supply	Typical GPIO bank supply	1.71–3.6	1.2 core/1.2–3.3 IO	V
V_{IL}	Input low voltage	CMOS input	$\leq$ 0.3 × VDD	$\leq$ 0.3 × VCCIO	V
V_{IH}	Input high voltage	CMOS input	$\geq$ 0.7 × VDD	$\geq$ 0.7 × VCCIO	V
V_{OL}	Output low voltage	IOL max	$\leq$ 0.4	$\leq$ 0.4	V
V_{OH}	Output high voltage	IOH max	$\geq$ VDD – 0.4	$\geq$ VCCIO – 0.4	V
I_{IL}	Input leakage current	GPIO input	$\pm$1	$\pm$10	uA
I_{OH}	Output source current	Per GPIO	~8	~8	mA
I_{OL}	Output sink current	Per GPIO	~8	~8	mA
RPU	Internal pull-up resistor	Typical	30–50	~100	kΩ
RPD	Internal pull-down resistor	Typical	30–50	~100	kΩ
FT	5V tolerant inputs	Selected GPIOs only	Yes	No	-
OD	Open-drain support	GPIO mode	Yes	Via logic / RGB pins native	-
Differential I/O	LVDS support	Differential pairs	Limited	Yes	-
Schmitt Trigger	Input hysteresis	GPIO input	Yes	Limited	-
Slew Control	Configurable output slew	GPIO output	Yes	Yes	-
Drive Strength	Configurable	GPIO output	Yes	Yes	-

Table 7: Recommended DC operating values

Please be aware that the FPGA pins are not 5V tolerant. Nonetheless, most MCU pins are 5V tolerant. Please refer to the respective datasheet for more information regarding pin and power characteristics.

State	Current
Standby	60 mA
Run (MCU)	100 mA
Run (MCU + Ethernet)	280 mA
Run (MCU + FPGA)	115 mA
Run (MCU + FPGA + Ethernet)	500 mA

Table 8: Power states (estimated values).

The values in 8 are provided for reference only. Actual power consumption may vary between modules.

5.2 Thermal

XIPHOS modules are specified for industrial environments where thermal, mechanical, and electrical stress are higher than in typical commercial applications. All variants support an operating temperature range starting at -40 °C; the upper limit depends on the variant (85 °C for XIPHOS-X1, 125 °C for XIPHOS-X2, and 140 °C for XIPHOS-X3 and XIPHOS-X4). These limits assume that the module is used within the specified supply and interface conditions and that adequate cooling or thermal coupling is provided when the system runs at high load for extended periods.

5.3 Mechanical

The XIPHOS module has a small footprint of 55mm × 40 mm. With the Phantom Forge case, the module measures 57.6mm × 42.6mm. The module features 4 M2.2 holes on each corner for mounting. The PCB thickness is 1.6mm ± 10%. Final height (with components) is 5.6mm. The Figure 1 shows the mechanical drawing of the XIPHOS with its most relevant dimensions. All measurements are in mm.

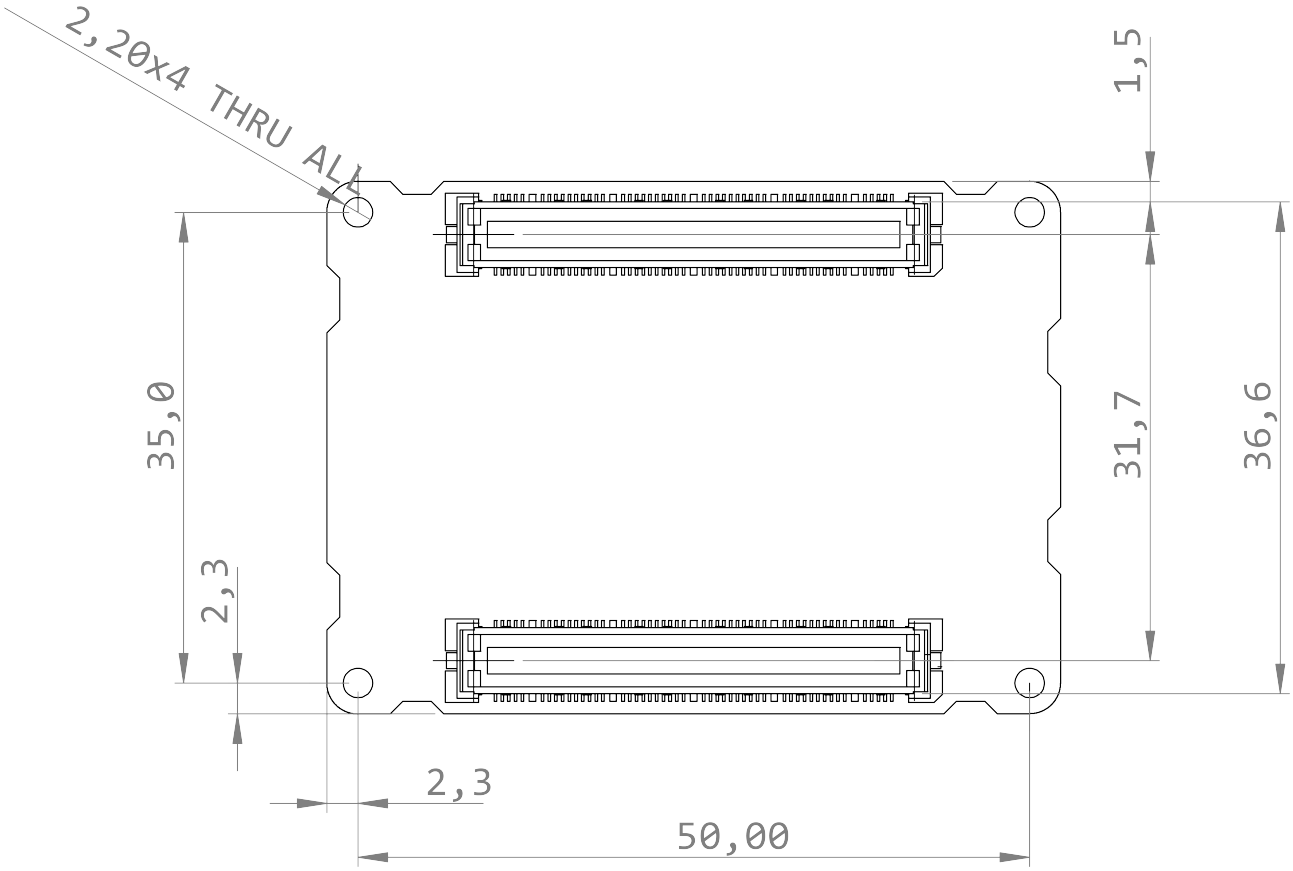

Figure 1: Bottom mechanical drawing of the XIPHOS X1/X2/X3/X4

There must be at least 2mm of clearance between the XIPHOS and the carrier board for successful mating. For information on the connectors, please refer to the FX11LA-100S/10-SV(92).

6 Pinout

XIPHOS exposes I/O through two 100-pin connector strips (J1 and J2), using Hirose FX11LA-100/10. Use the diagram and tables below for carrier-board design. Many signals are multifunction (GPIO, SPI, I²C, UART, CAN, SDMMC, Ethernet, USB, debug). Pins are not 5 V tolerant unless explicitly stated.[1]

6.1 J1 connector (100 pins)

Pin	Signal	Pin	Signal
J1-001	VDD	J1-002	IOB_8A
J1-003	VDD	J1-004	RAM_SIO3
J1-005	GND	J1-006	RAM_SIO2
J1-007	USB_DN	J1-008	RAM_MISO
J1-009	USB_DP	J1-010	RAM_MOSI
J1-011	VIN	J1-012	RAM_SCK
J1-013	VIN	J1-014	IOB_5B
J1-015	GND	J1-016	IOB_3B_G6
J1-017	FPGA_+3V3	J1-018	IOT_49A
J1-019	FPGA_+3V3	J1-020	IOT_51A
J1-021	GND	J1-022	GND
J1-023	FPGA_+1V2	J1-024	#LED_RGB2
J1-025	FPGA_+1V2	J1-026	#LED_RGB1
J1-027	GND	J1-028	#LED_RGB0
J1-029	FPGA_EN	J1-030	IOT_50B
J1-031	FPGA_EN	J1-032	IOT_45A_G1
J1-033	GND	J1-034	GND
J1-035	DONE	J1-036	IOT_48B
J1-037	GND	J1-038	IOT_46B_G0
J1-039	ETH_PWR_EN	J1-040	GND
J1-041	GND	J1-042	IOT_44B
J1-043	GPIO_14	J1-044	IOT_43A
J1-045	GPIO_15	J1-046	GND
J1-047	I2C2_SDA	J1-048	IOT_42B
J1-049	I2C2_SCL	J1-050	IOT_41A
J1-051	N.C.	J1-052	IOT_38B
J1-053	GND	J1-054	IOT_39A
J1-055	GND	J1-056	GND
J1-057	GND	J1-058	IOT_36B
J1-059	SPI5_MOSI	J1-060	IOT_37A
J1-061	SPI5_MISO	J1-062	GND
J1-063	GPIO_11	J1-064	#RAM_CS3
J1-065	SPI5_SCK	J1-066	#RAM_CS2
J1-067	SPI4_MOSI	J1-068	#RAM_CS1
J1-069	SPI4_MISO	J1-070	GND
J1-071	GPIO_3	J1-072	#RAM_CS0
J1-073	SPI4_SCK	J1-074	FPGA_SI
J1-075	SPI1_MOSI	J1-076	GND
J1-077	N.C.	J1-078	#FPGA_CS

[1] Note: In order for the XIPHOS to work please make sure all the GND pins are correctly connected.

Pin	Signal	Pin	Signal
J1-079	N.C.	J1-080	FPGA_SCK
J1-081	N.C.	J1-082	GND
J1-083	N.C.	J1-084	FPGA_SO
J1-085	N.C.	J1-086	8SPI_P1_IO3
J1-087	N.C.	J1-088	8SPI_P1_IO2
J1-089	N.C.	J1-090	8SPI_P1_IO4
J1-091	SPI2_MOSI	J1-092	8SPI_P1_IO5
J1-093	SPI2_MISO	J1-094	8SPI_P1_IO6
J1-095	SPI2_CLK	J1-096	8SPI_P1_IO7
J1-097	CAN3_RX	J1-098	C_DONE
J1-099	CAN3_TX	J1-100	#C_RESET

6.2 J2 connector (100 pins)

Pin	Signal	Pin	Signal
J2-001	N.C.	J2-002	POWER_EN
J2-003	GND	J2-004	UART7_RX
J2-005	VDD	J2-006	UART7_TX
J2-007	I2C1_SCL	J2-008	VIN
J2-009	I2C1_SDA	J2-010	CONN_ERR
J2-011	GPIO_7	J2-012	CONN_ERR
J2-013	SPI1_CLK	J2-014	VIN
J2-015	VDD	J2-016	VIN
J2-017	VDD	J2-018	VIN
J2-019	I2C2_SDA	J2-020	VIN
J2-021	I2C2_SCL	J2-022	VIN
J2-023	VDD	J2-024	VIN
J2-025	SPI1_MISO	J2-026	VDD
J2-027	N.C.	J2-028	#RESET
J2-029	SDMMC1_D6	J2-030	GND
J2-031	SDMMC1_D7	J2-032	SDMMC1_D2
J2-033	SDMMC1_D4	J2-034	SDMMC1_D1
J2-035	GND	J2-036	GND
J2-037	SDMMC1_D5	J2-038	SDMMC1_D0
J2-039	SDMMC1_CMD	J2-040	SDMMC1_D3
J2-041	GND	J2-042	GND
J2-043	GPIO_2	J2-044	SDMMC1_CK
J2-045	GPIO_3	J2-046	GPIO_13
J2-047	GPIO_4	J2-048	GPIO_9
J2-049	GPIO_5	J2-050	GPIO_8
J2-051	UART8_RX	J2-052	GND
J2-053	UART8_TX	J2-054	DBG_JTMS
J2-055	GND	J2-056	GND
J2-057	CAN2_RX	J2-058	DBG_JTCK
J2-059	CAN2_TX	J2-060	GND
J2-061	GND	J2-062	DBG_JTDO
J2-063	I2C4_SDA	J2-064	GND
J2-065	GND	J2-066	DBG_JTDI

Pin	Signal	Pin	Signal
J2-067	I2C4_SCL	J2-068	GND
J2-069	GND	J2-070	DBG_NRST
J2-071	8SPI_P1_IO2	J2-072	8SPI_P1_IO1
J2-073	8SPI_P1_IO3	J2-074	8SPI_P1_IO0
J2-075	8SPI_P1_IO4	J2-076	8SPI_P1_DQS
J2-077	8SPI_P1_IO5	J2-078	8SPI_P1_NCS
J2-079	8SPI_P1_IO6	J2-080	8SPI_P1_CLK
J2-081	8SPI_P1_IO7	J2-082	GND
J2-083	RMII_MDINT	J2-084	USB_VBUS
J2-085	ETH_PPS_OUT	J2-086	USB_ID
J2-087	ETH_LED2	J2-088	N.C.
J2-089	ETH_LED1	J2-090	N.C.
J2-091	ETH_2P	J2-092	ETH_1N
J2-093	ETH_2N	J2-094	ETH_1P
J2-095	ETH_3P	J2-096	ETH_0N
J2-097	ETH_3N	J2-098	ETH_0P
J2-099	GND	J2-100	GND

6.3 Pin description

Pin	Signal	Description
J1-001	VDD	+3V3 XIPHOS PMIC Output
J1-002	IOB_8A	General-purpose FPGA I/O
J1-003	VDD	+3V3 XIPHOS PMIC Output
J1-004	RAM_SIO3	RAM data bit 3 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_9B pin)
J1-005	GND	Ground (0V)
J1-006	RAM_SIO2	RAM data bit 2 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_6A pin)
J1-007	USB_DN	MCU USB Differential data line minus
J1-008	RAM_MISO	RAM data bit 1 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_4A pin)
J1-009	USB_DP	MCU USB Differential data line plus
J1-010	RAM_MOSI	RAM data bit 0 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_2A pin)
J1-011	VIN	+5V Main power input
J1-012	RAM_SCK	RAM serial clock (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_0A pin)
J1-013	VIN	+5V Main power input
J1-014	IOB_5B	General-purpose FPGA I/O
J1-015	GND	Ground (0V)
J1-016	IOB_3B_G6	General-purpose FPGA I/O
J1-017	FPGA_+3V3	+3V3 FPGA Output (Independent from PMIC +3V3). This pin gives the option of powering on / off the FPGA. It also applies power to the RAM modules.
J1-018	IOT_49A	General-purpose FPGA I/O
J1-019	FPGA_+3V3	+3V3 FPGA Output (Independent from PMIC +3V3). This pin gives the option of powering on / off the FPGA. It also applies power to the RAM modules.
J1-020	IOT_51A	General-purpose FPGA I/O
J1-021	GND	Ground (0V)
J1-022	GND	Ground (0V)
J1-023	FPGA_+1V2	+1V2 FPGA Output
J1-024	#LED_RGB2	LED2 sink/ general purpose FPGA I/O. Active low.
J1-025	FPGA_+1V2	+1V2 FPGA Output
J1-026	#LED_RGB1	LED1 sink/ general purpose FPGA I/O. Active low.
J1-027	GND	Ground (0V)
J1-028	#LED_RGB0	LED0 sink/ general purpose FPGA I/O. Active low.
J1-029	FPGA_EN	Enable PFGA power pin
J1-030	IOT_50B	General-purpose FPGA I/O
J1-031	FPGA_EN	Enable FPGA power pin
J1-032	IOT_45A_G1	General-purpose FPGA I/O
J1-033	GND	Ground (0V)
J1-034	GND	Ground (0V)
J1-035	DONE	FPGA pin. This pin goes high when the FPGA is correctly configured (Connected to pin PG2 in MCU).
J1-036	IOT_48B	General-purpose FPGA I/O
J1-037	GND	Ground (0V)
J1-038	IOT_46B_G0	General-purpose FPGA I/O

Pin	Signal	Description
J1-039	ETH_PWR_EN	MCU pin for enabling power to the Ethernet circuit
J1-040	GND	Ground (0V)
J1-041	GND	Ground (0V)
J1-042	IOT_44B	General-purpose FPGA I/O
J1-043	GPIO_14	General purpose Input / Output 14
J1-044	IOT_43A	General-purpose FPGA I/O
J1-045	GPIO_15	General purpose Input / Output 15
J1-046	GND	Ground (0V)
J1-047	I2C2_SDA	MCU Serial data 2- bidirectional, open-drain with pull-up
J1-048	IOT_42B	General-purpose FPGA I/O
J1-049	I2C2_SCL	MCU Serial Clock 2 - driven by master(s), open-drain with pull-up
J1-050	IOT_41A	General-purpose FPGA I/O
J1-051	N.C.	Not Connected
J1-052	IOT_38B	General-purpose FPGA I/O
J1-053	GND	Ground (0V)
J1-054	IOT_39A	General-purpose FPGA I/O
J1-055	GND	Ground (0V)
J1-056	GND	Ground (0V)
J1-057	GND	Ground (0V)
J1-058	IOT_36B	General-purpose FPGA I/O
J1-059	SPI5_MOSI	MCU SPI5 master output / slave input
J1-060	IOT_37A	General-purpose FPGA I/O
J1-061	SPI5_MISO	MCU SPI5 master input / slave output
J1-062	GND	Ground (0V)
J1-063	GPIO_11	General purpose Input / Output 11
J1-064	#RAM_CS3	Chip select for RAM 3 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_23B pin)
J1-065	SPI5_SCK	MCU SPI5 serial clock
J1-066	#RAM_CS2	Chip select for RAM 2 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_25B pin)
J1-067	SPI4_MOSI	MCU SPI4 master output / slave input
J1-068	#RAM_CS1	Chip select for RAM 1 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_29B pin)
J1-069	SPI4_MISO	MCU SPI4 master input / slave output
J1-070	GND	Ground (0V)
J1-071	GPIO_3	General purpose Input / Output 3
J1-072	#RAM_CS0	Chip select for RAM 0 (This pin is only available in XIPHOS X2 & X4; alt versions feature the FPGA General-purpose FPGA I/O IOB_31B pin)
J1-073	SPI4_SCK	MCU SPI1 serial clock
J1-074	FPGA_SI	FPGA slave input. This pin is allows SPI communication between the MCU and flash memory. We recommend not using this pin for external communication.
J1-075	SPI1_MOSI	MCU SPI1 master output / slave input
J1-076	GND	Ground (0V)
J1-077	N.C.	Not Connected
J1-078	#FPGA_CS	FPGA chip select. This pin is allows SPI communication between the MCU and flash memory. We recommend not using this pin for external communication.
J1-079	N.C.	Not Connected

Pin	Signal	Description
J1-080	FPGA_SCK	FPGA serial clock. This pin is allows SPI communication between the MCU and flash memory. We recommend not using this pin for external communication.
J1-081	N.C.	Not Connected
J1-082	GND	Ground (0V)
J1-083	N.C.	Not Connected
J1-084	FPGA_SO	FPGA slave output. This pin is allows SPI communication between the MCU and flash memory. We recommend not using this pin for external communication.
J1-085	N.C.	Not Connected
J1-086	OctoSPI_P1_IO3	MCU OctoSPIP1 Data bit 3
J1-087	N.C.	Not Connected
J1-088	OctoSPI_P1_IO2	MCU OctoSPIP1 Data bit 2
J1-089	N.C.	Not Connected
J1-090	OctoSPI_P1_IO4	MCU OctoSPIP1 Data bit 4
J1-091	SPI2_MOSI	MCU SPI master output / slave input
J1-092	OctoSPI_P1_IO5	MCU OctoSPIP1 Data bit 5
J1-093	SPI2_MISO	MCU SPI2 master input / slave output
J1-094	OctoSPI_P1_IO6	MCU OctoSPIP1 Data bit 6
J1-095	SPI2_CLK	MCU SPI2 Clock
J1-096	OctoSPI_P1_IO7	MCU OctoSPIP1 Data bit 7
J1-097	CAN3_RX	MCU CAN3 Receiver
J1-098	C_DONE	FPGA pin. This pin goes high when the FPGA is correctly configured(Connected to pin PG2 in MCU).
J1-099	CAN3_TX	MCU CAN3 Transmitter
J1-100	#C_RESET	FPGA reset pin
J2-001	N.C.	Not Connected
J2-002	POWER_EN	Enable pin for internal PMIC
J2-003	GND	Ground (0V)
J2-004	UART7_RX	MCU UART7 Receiver
J2-005	VDD	+3V3 XIPHOS output
J2-006	UART7_TX	MCU UART7 Transmitter
J2-007	I2C1_SCL	MCU Serial Clock 1 - driven by master(s), open-drain with pull-up
J2-008	VIN	+5V main power input
J2-009	I2C1_SDA	MCU Serial data 1 - bidirectional, open-drain with pull-up
J2-010	CONN_ERR	Pin for ensuring correct placement of XIPHOS in CarrierBoard. Do not connect anything to this pin.
J2-011	GPIO_7	General purpose Input / Output 7
J2-012	CONN_ERR	Pin for ensuring correct placement of XIPHOS in CarrierBoard. Do not connect anything to this pin.
J2-013	SPI1_CLK	Serial Clock - driven by master(s), open-drain with pull-up
J2-014	VIN	+5V Main power input
J2-015	VDD	+3V3 XIPHOS Output
J2-016	VIN	+5V Main power input
J2-017	VDD	+3V3 XIPHOS Output
J2-018	VIN	+5V Main power input
J2-019	I2C2_SDA	MCU Serial data 2 - bidirectional, open-drain with pull-up
J2-020	VIN	+5V Main power input
J2-021	I2C2_SCL	MCU Serial Clock 2 - driven by master(s), open-drain with pull-up
J2-022	VIN	+5V Main power input

Pin	Signal	Description
J2-023	VDD	+3V3 XIPHOS Output
J2-024	VIN	+5V Main power input
J2-025	SPI1_MISO	MCU SPI1 master in, slave out
J2-026	VDD	+3V3 XIPHOS Output
J2-027	N.C.	Not Connected
J2-028	#RESET	System reset, active low
J2-029	SDMMC1_D6	MCU SDMMC1 Data bit 6
J2-030	GND	Ground (0V)
J2-031	SDMMC1_D7	MCU SDMMC1 Data bit 7
J2-032	SDMMC1_D2	MCU SDMMC1 Data bit 2
J2-033	SDMMC1_D4	MCU SDMMC1 Data bit 4
J2-034	SDMMC1_D1	MCU SDMMC1 Data bit 1
J2-035	GND	Ground (0V)
J2-036	GND	Ground (0V)
J2-037	SDMMC1_D5	MCU SDMMC1 Data bit 5
J2-038	SDMMC1_D0	MCU SDMMC1 Data bit 0
J2-039	SDMMC1_CMD	MCU SDMMC1 Command / response line
J2-040	SDMMC1_D3	MCU SDMMC1 Data bit 3
J2-041	GND	Ground (0V)
J2-042	GND	Ground (0V)
J2-043	GPIO_2	General purpose Input / Output 2
J2-044	SDMMC1_CK	MCU SDMMC1 Clock from host
J2-045	GPIO_3	General purpose Input / Output 3
J2-046	GPIO_13	General purpose Input / Output 13
J2-047	GPIO_4	General purpose Input / Output 4
J2-048	GPIO_9	General purpose Input / Output 9
J2-049	GPIO_5	General purpose Input / Output 5. Pin connected to built-in LED
J2-050	GPIO_8	General purpose Input / Output 8
J2-051	UART8_RX	MCU UART8 Receiver
J2-052	GND	Ground (0V)
J2-053	UART8_TX	MCU UART8 Transmitter
J2-054	DBG_JTMS	MCU Bidirectional data (SWD) / TAP state machine control (JTAG)
J2-055	GND	Ground (0V)
J2-056	GND	Ground (0V)
J2-057	CAN2_RX	MCU CAN2 Receiver
J2-058	DBG_JTCK	MCU Serial Wire Debug / JTAG Clock
J2-059	CAN2_TX	MCU CAN2 Transmitter
J2-060	GND	Ground (0V)
J2-061	GND	Ground (0V)
J2-062	DBG_JTDO	MCU Serial wire output trace (SWD) / scan data out (JTAG)
J2-063	I2C4_SDA	MCU Serial data 4 - bidirectional, open-drain with pull-up
J2-064	GND	Ground (0V)
J2-065	GND	Ground (0V)
J2-066	DBG_JTDI	MCU JTAG only - scan data in
J2-067	I2C4_SCL	MCU Serial Clock 4 - driven by master(s), open-drain with pull-up
J2-068	GND	Ground (0V)
J2-069	GND	Ground (0V)
J2-070	DBG_NRST	MCU Serial Wire Debug / JTAG Reset
J2-071	OctoSPI_P1_IO2	MCU OctoSPIP1 Data bit 2
J2-072	OctoSPI_P1_IO1	MCU OctoSPIP1 Data bit 1

Pin	Signal	Description
J2-073	OctoSPI_P1_IO3	MCU OctoSPIP1 Data bit 3
J2-074	OctoSPI_P1_IO0	MCU OctoSPIP1 Data bit 0
J2-075	OctoSPI_P1_IO4	MCU OctoSPIP1 Data bit 4
J2-076	OctoSPI_P1_DQS	MCU OctoSPIP1 Data strobe — used in DTR mode for read data latching; can also be used as RWDS (Read/Write Data Strobe) in HyperBus
J2-077	OctoSPI_P1_IO5	MCU OctoSPIP1 Data bit 5
J2-078	OctoSPI_P1_NCS	MCU OctoSPIP1 Chip select, active low — enables the target device
J2-079	OctoSPI_P1_IO6	MCU OctoSPIP1 Data bit 6
J2-080	OctoSPI_P1_CLK	MCU OctoSPIP1 Serial clock — drives data sampling on the memory side
J2-081	OctoSPI_P1_IO7	MCU OctoSPIP1 Data bit 7
J2-082	GND	Ground (0V)
J2-083	RMII_MDINT	Ethernet management data input / output
J2-084	USB_VBUS	+5V supply from host (or VBUS detect only in device mode)
J2-085	ETH_PPS_OUT	Ethernet pulse per second output
J2-086	USB_ID	MCU USB OTG mode detection
J2-087	ETH_LED2	Active-Low ethernet activity indicator
J2-088	N.C.	Not Connected
J2-089	ETH_LED1	Active-Low ethernet activity indicator
J2-090	N.C.	Not Connected
J2-091	ETH_2P	Ethernet pair 2 positive (connect to transformer or MagJack)
J2-092	ETH_1N	Ethernet pair 1 negative (connect to transformer or MagJack)
J2-093	ETH_2N	Ethernet pair 2 negative (connect to transformer or MagJack)
J2-094	ETH_1P	Ethernet pair 1 positive (connect to transformer or MagJack)
J2-095	ETH_3P	Ethernet pair 3 positive (connect to transformer or MagJack)
J2-096	ETH_0N	Ethernet pair 0 negative (connect to transformer or MagJack)
J2-097	ETH_3N	Ethernet pair 3 negative (connect to transformer or MagJack)
J2-098	ETH_0P	Ethernet pair 0 positive (connect to transformer or MagJack)
J2-099	GND	Ground (0V)
J2-100	GND	Ground (0V)

For more information regarding specific MCU or FPGA pins, please refer to the STM32H735xG or the ICE40UP5K datasheet.

6.4 Pinout diagram

The following pages show the connector pinout (J1 and J2) as a diagram. Signal names, power (VDD, VIN, GND), and function groups match the tables above.

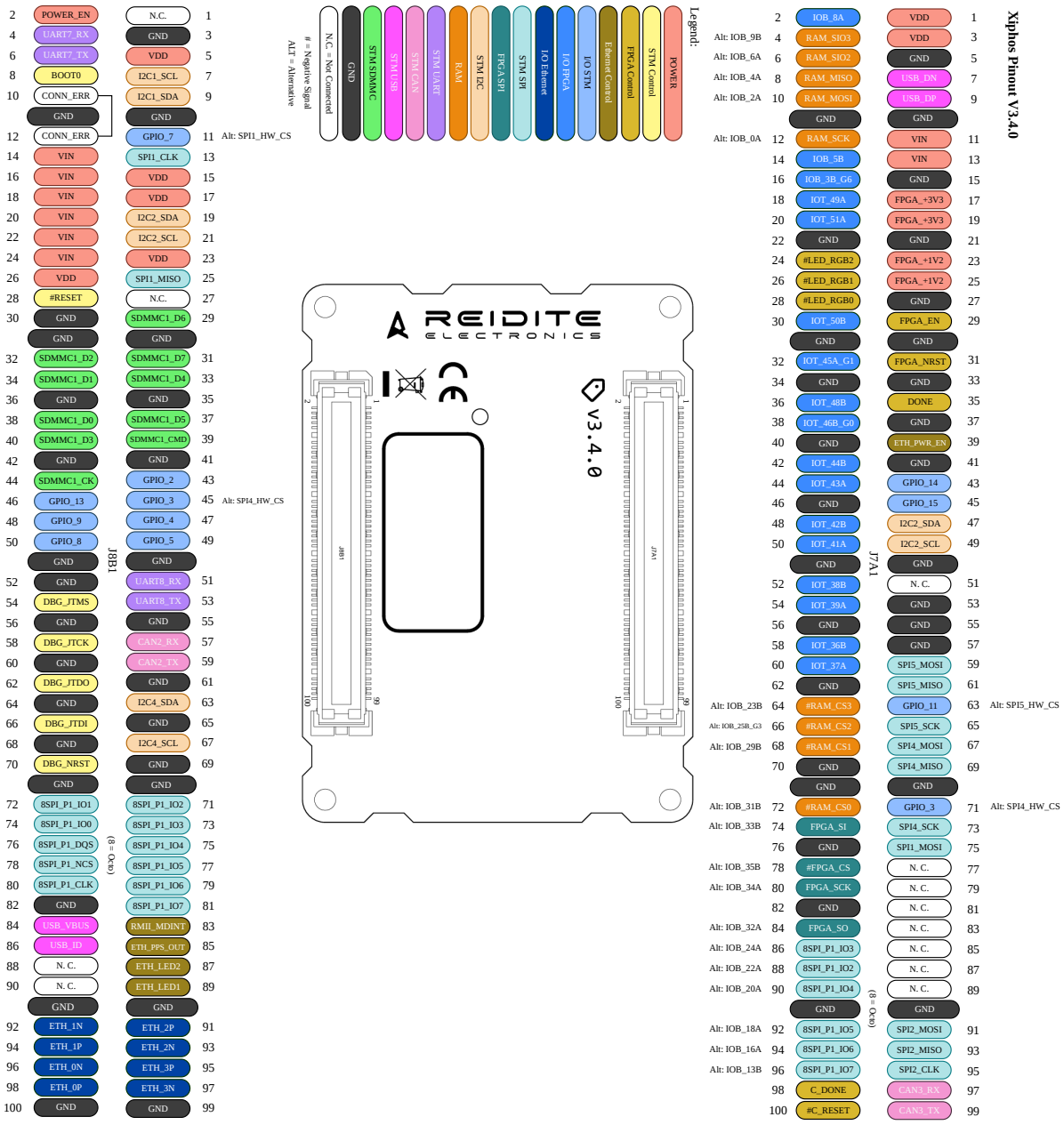

Figure 2: Pinout diagram with color-coded legend.

7 Power

XIPHOS requires a single +5V supply with at least 600mA to work to its full potential. The TPS62132RGTR power regulator supplies the whole system. The FPGA and Ethernet modules have their own proprietary voltage regulators with enable pins controlled by the MCU. This helps with power efficiency when certain modules are not required. When power is applied, the MCU is the first to wake up. Then, based on the selection in the firmware package, the rest of the system is powered on. Please refer to our product page for our latest XIPHOS software revision.

Note:

When powering off, please make sure all power has been disconnected from the module.

8 Troubleshooting

8.1 Module does not power up or show signs of life

- Check that the carrier supplies a stable 5V within the specified current capability and that polarity is correct.
- Verify that the module is fully seated on both connectors (J1 and J2).
- Inspect the connector area for bent pins, contamination, or damage.
- Confirm that the carrier board schematic matches the XIPHOS pinout (power and ground pins in particular).

8.2 Debugger cannot connect (MCU)

- Ensure SWD/JTAG lines (and VDD, GND if required by the probe) are correctly routed from the carrier to the debug connector.
- Check that no other driver or application is holding the debug interface (close other IDEs or tools).
- Try a power cycle: remove power, wait a few seconds, then reapply and retry the connection.
- If the MCU was set to disable the debug port, use the bootloader (e.g. USB-DFU or UART) to recover or re-enable debug access as per the product documentation.

8.3 FPGA does not configure

- Verify JTAG connectivity and that the correct voltage levels are used for the FPGA I/O.
- If the bitstream is loaded by the MCU at boot, ensure the MCU firmware has loaded the correct image and that the storage (e.g. Flash) is accessible and intact.
- Check the Models Datasheet for the recommended configuration flow (JTAG vs MCU-loaded).

8.4 Ethernet or other interfaces not working

- Confirm pin mapping and alternate function configuration in your firmware and carrier design.
- For Ethernet, ensure the PHY is powered and that RMII signals are routed with correct impedance and length matching.
- Review the electrical and operating conditions; ensure the module is within the specified temperature and supply limits.

8.5 Where to get help

For further support, contact REIDITE Industries with your module variant, carrier description, and a concise description of the symptom and steps already tried. Refer to the ordering section in the Family Datasheet for contact information.

9 Disclaimer

This document is released as version v1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Industries website and the XIPHOS product page (downloads). For the latest specifications, always refer to the official datasheets and the REIDITE Industries website.