XIPHOS Models

Model-specific specifications

XIPHOS-X1 / XIPHOS-X2 / XIPHOS-X3 / XIPHOS-X4

v1.0

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1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2025-02-02	Release 1.0 for distribution.
v1.1	2026-01-26	Pinout updated from official diagram; diagram embedded in Models datasheet; new Pinout reference document added.

2 Hardware version guide

This documentation applies to XIPHOS hardware version **3.2.0**. Ensure that your module and carrier design match this revision; for other hardware versions, contact REIDITE Electronics or refer to the XIPHOS product page (downloads).

Contents

List of Figures

List of Tables

3 Summary

This document details the XIPHOS-X1, XIPHOS-X2, XIPHOS-X3, and XIPHOS-X4 variants of the XIPHOS family. All models share the same base architecture: an STM32H7 microcontroller, a Lattice iCE40 UltraPlus FPGA, and an integrated Ethernet PHY. The main differences between variants are packaging (open-frame versus Phantom Forge® encapsulation), maximum operating temperature, and the presence or absence of external PSRAM. This consistency allows a single software and hardware baseline to cover the full range, with drop-in upgrades when higher temperature or memory headroom is required.

The module exposes I/O through two 100-pin board-to-board connectors (Hirose FX11LA-100/10). These provide general-purpose signals and industrial interfaces, including SPI, I^2C, UART, GPIO, Ethernet, USB, and CAN FD, as well as FPGA-programmable pins. The electrical mapping and pinout are **consistent across XIPHOS-X1–XIPHOS-X4**, so one carrier board design can support all variants.

XIPHOS modules are assembled in qualified environments with controlled residue management to avoid contamination in industrial systems. **All XIPHOS models are RoHS free.** The MCU + FPGA architecture delivers deterministic real-time control and hardware flexibility without the complexity of a Linux-based SoC, making it suitable for industrial automation, motor control, and connectivity-heavy edge applications.

4 MCU details (STM32H735IGT)

The industrial processor at the heart of every XIPHOS module is the STM32H735IGT from STMicroelectronics. This 32-bit ARM Cortex-M7 device delivers deterministic real-time performance with a dual-bank internal Flash architecture and hardware cryptographic acceleration, making it suitable for safety-conscious and connectivity-heavy applications without resorting to a Linux-based SoC.

The Cortex-M7 core runs at up to 550 MHz with a double-precision FPU and optional DSP instructions. Instruction and data caches (32 KB each) reduce latency when executing from external Flash or when accessing frequently used data, while tightly coupled memory (TCM) provides predictable access times for time-critical code and data. The MCU integrates 1 MB of internal Flash with ECC and approximately 564 KB of internal SRAM (TCM, AXI SRAM, and DTCM), allowing substantial application and RTOS footprint without depending solely on external memories.

On the connectivity side, the STM32H735 provides an Ethernet MAC (with RMII/RGMII support depending on carrier design), USB 2.0 OTG, multiple CAN FD controllers, high-resolution ADCs, and a rich set of timers. Hardware cryptographic accelerators and a true random number generator (RNG) support secure boot, secure firmware updates, and encrypted communications. FreeRTOS and other real-time operating systems are commonly used to structure the application and to isolate critical tasks from non-critical ones.

The external 8 MB Flash on the module complements the MCU internal memory for firmware, configuration, and data logging. The on-chip boot ROM supports in-field updates without JTAG access via USB-DFU, UART, or other configured interfaces, enabling remote maintenance and reduced downtime in deployed systems.

4.1 Summary of key parameters

- **CPU:** ARM Cortex-M7 up to 550 MHz.
- **Internal Flash:** 1 MB with ECC.
- **Internal SRAM:** ~564 KB (TCM + AXI + DTCM).
- **Cache:** 32 KB I-Cache + 32 KB D-Cache.
- **Peripherals:** Ethernet MAC, USB 2.0 OTG, CAN FD, ADCs, timers, crypto accelerators, RNG.

- **RTOS support:** FreeRTOS and others.

5 FPGA details (ICE40UP5K-SG48I)

The programmable logic on each XIPHOS module is provided by a Lattice iCE40 UltraPlus device (part number ICE40UP5K-SG48I). This small-footprint FPGA sits between the MCU and the external I/O, enabling protocol adaptation, deterministic timing generation, and custom glue logic without adding a separate discrete ASIC or a more complex SoC. The industrial processor and the FPGA together form a flexible compute pair: the MCU runs the application and communication stack, while the FPGA handles time-critical or protocol-specific tasks with predictable latency.

The iCE40 UltraPlus offers approximately 5280 4-input LUTs with associated flip-flops and about 120 kbit of embedded block RAM. In XIPHOS, the FPGA is typically used at clock rates below 50 MHz, which keeps power and signal-integrity margins comfortable while still supporting real-time interfaces such as custom serial protocols, pulse generation, or multiplexed I/O expansion. The core voltage is nominally 1.2 V; the exact number of user I/O pins available depends on the package and the integration with the MCU and connectors.

Typical XIPHOS usage includes protocol adaptation (e.g. translating between legacy industrial buses and the MCU), deterministic timing generation for actuators or sensors, and custom I/O logic where sub-microsecond response is required. By offloading these functions to the FPGA, the MCU is freed to handle application logic, networking, and storage, while the FPGA ensures deterministic signal timing and precise control loops. The bitstream can be loaded by the MCU at boot or from external storage, allowing field updates of FPGA behaviour without physical access to the board.

5.1 Summary of key parameters

- **Family:** Lattice iCE40 UltraPlus.
- **Logic capacity:** ~5280 LUTs (4-LUT + FF).
- **Internal RAM:** ~120 kbit SRAM.
- **I/O count:** ~39 programmable pins (package dependent).
- **Typical frequency:** < 50 MHz (design dependent).
- **Core voltage:** ~1.2 V.

6 Programming and debug

XIPHOS supports both development-time debugging and production or in-field firmware updates. The MCU and FPGA can be programmed and debugged via standard interfaces; the choice of method depends on the development phase and whether physical access to the board is available.

6.1 MCU

The STM32H735 is programmed and debugged via SWD or JTAG using tools such as ST-LINK, J-Link, or OpenOCD. Development is typically done with STM32CubeIDE or STM32CubeMX for project setup and with GCC ARM and GDB for building and debugging. The MCU incorporates an on-chip bootloader in ROM that supports USB-DFU, UART, SPI, and CAN as entry points for firmware updates. Thus, in production or in the field, the application can be updated without JTAG access: the device is placed in bootloader mode (e.g. via a GPIO or a specific power-up sequence), and the new image is delivered over USB, UART, or another supported channel. This reduces dependency on debug connectors and simplifies deployment and maintenance.

- **Debug/programming:** SWD / JTAG (ST-LINK, J-Link, OpenOCD).
- **Bootloader:** USB-DFU, UART, SPI, CAN (internal ROM).
- **Tooling:** STM32CubeIDE / STM32CubeMX, GCC ARM + GDB.

6.2 FPGA

During development, the Lattice iCE40 FPGA is typically programmed via JTAG using Lattice iCEcube2 or Radiant, or with the open-source toolchain (Yosys, nextpnr, IceStorm). In production and in the field, the FPGA bitstream is often stored in external Flash or in the MCU filesystem and loaded by the MCU at boot. The MCU can verify the bitstream (e.g. with a checksum or signature) before configuring the FPGA, so that field updates of FPGA functionality are possible without physical access to the board. Document whether configuration is persistent in the FPGA or reloaded on each boot in your system integration flow, as this affects startup time and update procedures.

- **Development programming:** JTAG.
- **Production configuration:** bitstream loaded by the MCU at boot.
- **Toolchains:** Lattice iCEcube2 / Radiant, or open-source Yosys + nextpnr + IceStorm.

7 Connectors and carrier board

All I/O between the XIPHOS module and the carrier board is brought out through two 100-pin board-to-board connectors, **Hirose FX11LA-100/10**, designated J1 and J2. These connectors provide a dense, reliable interface for power, ground, and the full set of digital and analogue signals (SPI, I^2C, UART, GPIO, Ethernet, USB, CAN FD, and FPGA I/O). Carrier-board designers must use the vendor-recommended mating connector and footprint to guarantee mechanical fit, electrical contact, and long-term reliability.

Connector placement, orientation, and stack height are defined in the mechanical documentation. Validate your carrier layout against those drawings to ensure clearance, tolerance compliance, and correct mating sequence during assembly. Incorrect stack height or misalignment can lead to intermittent contacts or damage to the connectors.

JTAG and SWD pins are available on the connector for debug and factory programming. Many MCU and FPGA pins are multiplexed and require firmware or bitstream configuration to match the intended function; consult the pinout and application notes when assigning signals. Unless explicitly stated in the pinout, pins are not 5 V tolerant and must not be driven above the MCU or FPGA I/O voltage. For signal integrity, route Ethernet, USB, and clock signals with controlled impedance and minimise crosstalk with other high-speed or sensitive lines.

7.1 Integration notes

- JTAG/SWD pins are provided for debug and factory programming.
- Some pins are multiplexed and require firmware configuration.
- Pins are not 5 V tolerant unless explicitly stated.
- Route Ethernet, USB, and clock signals with controlled impedance.

8 Connector pinout

XIPHOS exposes I/O through two 100-pin connector strips (J1 and J2), using Hirose FX11LA-100/10. Use the diagram and tables below for carrier-board design. Many signals are multifunction (GPIO, SPI, I^2C, UART, CAN, SDMMC, Ethernet, USB, debug). Pins are not 5 V tolerant unless explicitly stated.

8.1 J1 connector (100 pins)

Pin	Signal	Pin	Signal
J1-001	N.C.	J1-002	GND
J1-003	VDD	J1-004	N.C.
J1-005	N.C.	J1-006	GND
J1-007	N.C.	J1-008	N.C.
J1-009	VDD	J1-010	VDD
J1-011	I2C2_SDA	J1-012	I2C2_SCL
J1-013	VDD	J1-014	N.C.
J1-015	VIN	J1-016	SDMMC1_D6
J1-017	GND	J1-018	SDMMC1_D7
J1-019	SDMMC1_D4	J1-020	GND
J1-021	SDMMC1_D5	J1-022	SDMMC1_CMD
J1-023	GND	J1-024	GPIO_2
J1-025	GPIO_3	J1-026	GPIO_4
J1-027	GPIO_5	J1-028	GND
J1-029	UART8_RX	J1-030	UART8_TX
J1-031	GND	J1-032	CAN2_RX
J1-033	CAN2_TX	J1-034	GND
J1-035	I2C4_SDA	J1-036	GND
J1-037	I2C4_SCL	J1-038	GND
J1-039	GND	J1-040	8SPI_P1_IO2
J1-041	8SPI_P1_IO3	J1-042	8SPI_P1_IO4
J1-043	8SPI_P1_IO5	J1-044	8SPI_P1_IO6
J1-045	8SPI_P1_IO7	J1-046	RMII_MDINT
J1-047	ETH_PPS_OUT	J1-048	ETH_LED2
J1-049	ETH_LED1	J1-050	GND
J1-051	ETH_2P	J1-052	ETH_2N
J1-053	ETH_3P	J1-054	ETH_3N
J1-055	GND	J1-056	GND
J1-057	ETH_0P	J1-058	ETH_0N
J1-059	ETH_1P	J1-060	ETH_1N
J1-061	GND	J1-062	USB_DP
J1-063	USB_DN	J1-064	USB_ID
J1-065	USB_VBUS	J1-066	GND
J1-067	8SPI_P1_CLK	J1-068	8SPI_P1_NCS
J1-069	8SPI_P1_DQS	J1-070	8SPI_P1_IO0
J1-071	8SPI_P1_IO1	J1-072	GND
J1-073	DBG_NRST	J1-074	GND
J1-075	DBG_JTDI	J1-076	GND
J1-077	DBG_SWO	J1-078	GND
J1-079	DBG_SWCLK	J1-080	GND
J1-081	DBG_SWDIO	J1-082	GND
J1-083	GND	J1-084	GPIO_8
J1-085	GPIO_9	J1-086	GPIO_13
J1-087	RESET	J1-088	VDD
J1-089	VIN	J1-090	VIN
J1-091	VIN	J1-092	VIN
J1-093	VIN	J1-094	N.C.
J1-095	GND	J1-096	N.C.

Pin	Signal	Pin	Signal
J1-097	BOOT0	J1-098	N.C.
J1-099	N.C.	J1-100	POWER_EN

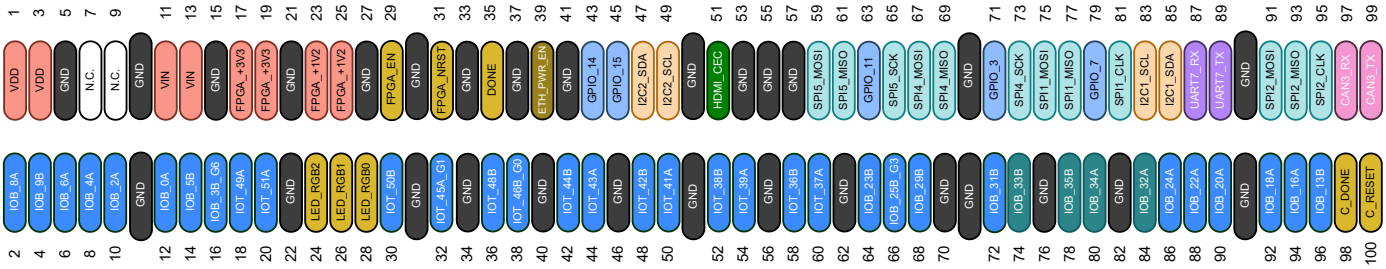
8.2 J2 connector (100 pins)

Pin	Signal	Pin	Signal
J2-001	VDD	J2-002	VDD
J2-003	GND	J2-004	N.C.
J2-005	N.C.	J2-006	GND
J2-007	VIN	J2-008	VIN
J2-009	GND	J2-010	FPGA_+3V3
J2-011	FPGA_+3V3	J2-012	GND
J2-013	FPGA_+1V2	J2-014	FPGA_+1V2
J2-015	GND	J2-016	FPGA_EN
J2-017	GND	J2-018	FPGA_NRST
J2-019	GND	J2-020	DONE
J2-021	GND	J2-022	ETH_PWR_EN
J2-023	GND	J2-024	GPIO_14
J2-025	GPIO_15	J2-026	I2C2_SDA
J2-027	I2C2_SCL	J2-028	GND
J2-029	HDMI_CEC	J2-030	GND
J2-031	GND	J2-032	GND
J2-033	SPI5_MOSI	J2-034	SPI5_MISO
J2-035	GPIO_11	J2-036	SPI5_SCK
J2-037	SPI4_MOSI	J2-038	SPI4_MISO
J2-039	GND	J2-040	GPIO_3
J2-041	SPI4_SCK	J2-042	SPI1_MOSI
J2-043	SPI1_MISO	J2-044	GPIO_7
J2-045	SPI1_CLK	J2-046	I2C1_SCL
J2-047	I2C1_SDA	J2-048	UART7_RX
J2-049	UART7_TX	J2-050	GND
J2-051	SPI2_MOSI	J2-052	SPI2_MISO
J2-053	SPI2_CLK	J2-054	CAN3_RX
J2-055	CAN3_TX	J2-056	C_RESET
J2-057	C_DONE	J2-058	IOB_13B
J2-059	IOB_16A	J2-060	IOB_18A
J2-061	GND	J2-062	IOB_20A
J2-063	IOB_22A	J2-064	IOB_24A
J2-065	IOB_32A	J2-066	GND
J2-067	IOB_34A	J2-068	IOB_35B
J2-069	GND	J2-070	IOB_33B
J2-071	IOB_31B	J2-072	GND
J2-073	GND	J2-074	IOB_29B
J2-075	IOB_25B_G3	J2-076	IOB_23B
J2-077	GND	J2-078	IOT_37A
J2-079	IOT_36B	J2-080	GND
J2-081	IOT_39A	J2-082	IOT_38B
J2-083	GND	J2-084	IOT_41A

Pin	Signal	Pin	Signal
J2-085	IOT_42B	J2-086	GND
J2-087	IOT_43A	J2-088	IOT_44B
J2-089	GND	J2-090	IOT_46B_G0
J2-091	IOT_48B	J2-092	GND
J2-093	IOT_45A_G1	J2-094	GND
J2-095	IOT_50B	J2-096	LED_RGB0
J2-097	LED_RGB0	J2-098	LED_RGB1
J2-099	LED_RGB2	J2-100	GND

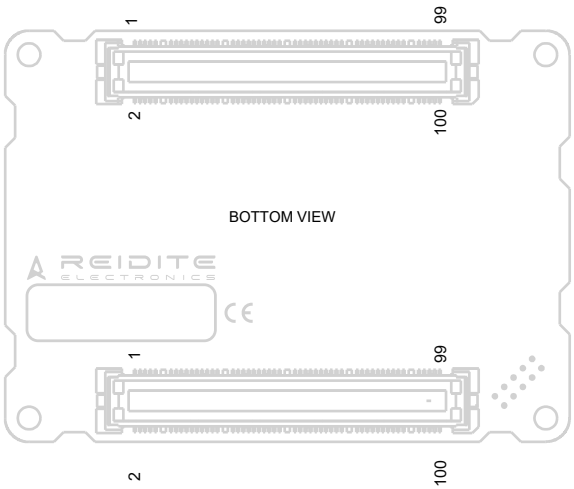
8.3 Pinout diagram

The following pages show the connector pinout (J1 and J2) as a diagram. Signal names, power (VDD, VIN, GND), and function groups match the tables above.



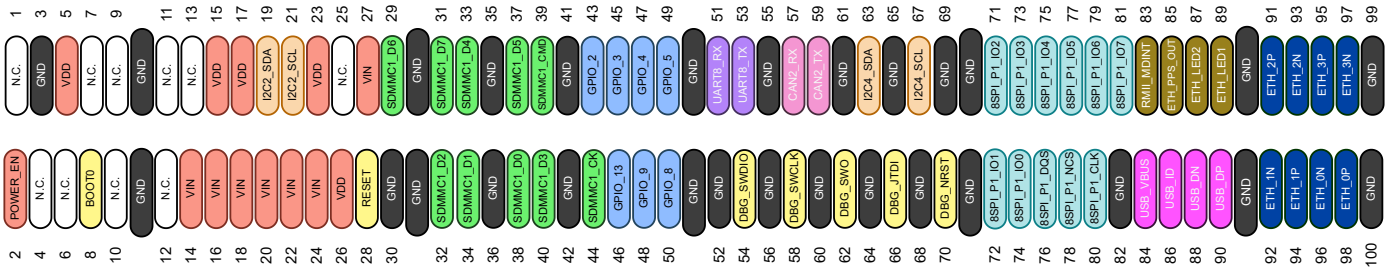
Leyenda:

- POWER
- STM Control
- FPGA Control
- Ethernet Control
- I/O STM
- I/O FPGA
- I/O Ethernet
- STM SPI
- FPGA SPI
- STM I2C
- FPGA I2C
- STM UART
- STM CAN
- STM USB
- STM SDMMC
- STM HDMI
- GND
- N.C. = Not Connected



Función

Pin | Principal | Alternativa



9 Comparison table

The following table provides a side-by-side comparison of the four XIPHOS variants. It summarises the main differences in packaging (Phantom Forge®), memory (PSRAM), and operating temperature so that the right model can be selected for each application. All variants share the same MCU, FPGA, and pinout.

Feature	XIPHOS-X1	XIPHOS-X2	XIPHOS-X3	XIPHOS-X4
Phantom Forge®	No	No	Yes	Yes
MCU (model)	STM32H735IGT	STM32H735IGT	STM32H735IGT	STM32H735IGT
MCU Flash (int.)	1 MB (ECC)	1 MB (ECC)	1 MB (ECC)	1 MB (ECC)
MCU SRAM (int.)	~564 KB	~564 KB	~564 KB	~564 KB
PSRAM (external)	None	32 MB	None	32 MB
Flash (external)	8 MB	8 MB	8 MB	8 MB
Lattice FPGA (model)	ICE40UP5K-SG48I	ICE40UP5K-SG48I	ICE40UP5K-SG48I	ICE40UP5K-SG48I
Ethernet PHY	Integrated	Integrated	Integrated	Integrated
Min temperature	-40 °C	-40 °C	-40 °C	-40 °C
Max temperature	85 °C	125 °C	140 °C	140 °C

Table 3: Comparison of XIPHOS-X1, XIPHOS-X2, XIPHOS-X3, and XIPHOS-X4.

RoHS free: all XIPHOS models.

TBD: to be defined based on the final configuration of each variant.

10 XIPHOS-X1

10.1 Description

The XIPHOS-X1 is the **base variant** of the family: a compact module combining the **STM32H735** MCU and the **Lattice iCE40 UltraPlus** FPGA without Phantom Forge® encapsulation. It is designed for integration into **controlled environments** or into carrier boards and enclosures that already provide mechanical support, thermal management, and environmental protection. The XIPHOS-X1 offers the same processing and connectivity capabilities as the rest of the family (**Ethernet**, USB, CAN FD, programmable FPGA I/O) with a lower maximum operating temperature and without external PSRAM, making it suitable for cost-sensitive or space-constrained applications where moderate thermal and memory requirements are sufficient.

10.2 Key specifications

The main electrical and thermal parameters for this variant are summarised below. Table 4 lists the key specifications for the XIPHOS-X1.

10.3 Notes

XIPHOS-X1 targets controlled environments where compact size and baseline functionality are prioritised. It is suitable for applications with moderate thermal requirements, such as indoor industrial equipment, lab instruments, or embedded systems inside a protected enclosure. For harsher conditions or higher memory needs, consider the XIPHOS-X2 (open-frame with PSRAM and higher temperature), XIPHOS-X3 (encapsulated), or XIPHOS-X4 (encapsulated with PSRAM).

Parameter	Value
STM32 MCU	STM32H735IGT
MCU Flash (internal)	1 MB (ECC)
MCU SRAM (internal)	~564 KB
PSRAM (external)	None
Flash (external)	8 MB
Lattice FPGA	ICE40UP5K-SG48I
Min temperature	-40 °C
Max temperature	85 °C

Table 4: Key specifications for XIPHOS-X1.

11 XIPHOS-X2

11.1 Description

The XIPHOS-X2 is an **expanded open-frame** variant that adds **32 MB** of external PSRAM and a higher maximum operating temperature (**125 °C**) while retaining the same MCU, FPGA, and **connector pinout** as the XIPHOS-X1. It is intended for applications that need more RAM for larger buffers, protocol stacks, data logging, or edge processing, and for environments where ambient temperature or sustained high load would exceed the XIPHOS-X1 rating. Like the XIPHOS-X1, the XIPHOS-X2 is supplied without Phantom Forge® encapsulation, so it is intended for integration into carrier boards or enclosures that provide mechanical and environmental protection.

11.2 Key specifications

Below are the key specifications for this variant. Table 5 summarises the main parameters for the XIPHOS-X2, including the 32 MB external PSRAM and the extended temperature range.

Parameter	Value
STM32 MCU	STM32H735IGT
MCU Flash (internal)	1 MB (ECC)
MCU SRAM (internal)	~564 KB
PSRAM (external)	32 MB
Flash (external)	8 MB
Lattice FPGA	ICE40UP5K-SG48I
Min temperature	-40 °C
Max temperature	125 °C

Table 5: Key specifications for XIPHOS-X2.

11.3 Notes

XIPHOS-X2 adds memory headroom for larger buffers, protocol stacks, and data logging, and its higher maximum temperature rating supports extended industrial duty cycles in hot environments or in enclosures with limited cooling. It is a suitable step-up from the XIPHOS-X1 when more RAM or thermal margin is required without moving to an encapsulated variant. For harsh humidity or vibration, consider the

XIPHOS-X3 or XIPHOS-X4 with Phantom Forge® encapsulation.

12 XIPHOS-X3

12.1 Description

The XIPHOS-X3 is the base variant with **Phantom Forge® encapsulation**. It shares the same MCU, FPGA, and memory configuration as the XIPHOS-X1 (no external PSRAM) but is protected by the Phantom Forge® overmould, which improves resistance to humidity, dust, and mechanical stress and provides **IP66** ingress protection. The maximum operating temperature is **140 °C**, making the XIPHOS-X3 suitable for **demanding industrial environments** where open-frame boards would be at risk: high-vibration machinery, wash-down or outdoor-like conditions, or applications where long-term reliability under thermal and environmental stress is critical.

12.2 Key specifications

The main specifications for this encapsulated variant are listed below. Table 6 gives the key parameters for the XIPHOS-X3, including the Phantom Forge® encapsulation and the 140 °C maximum temperature.

Parameter	Value
STM32 MCU	STM32H735IGT
MCU Flash (internal)	1 MB (ECC)
MCU SRAM (internal)	~564 KB
PSRAM (external)	None
Flash (external)	8 MB
Lattice FPGA	ICE40UP5K-SG48I
Min temperature	-40 °C
Max temperature	140 °C

Table 6: Key specifications for XIPHOS-X3.

12.3 Notes

XIPHOS-X3 combines Phantom Forge® encapsulation with high-temperature capability for robust deployments in harsh industrial environments. It is the right choice when environmental or mechanical conditions rule out open-frame variants but when the application does not require the extra 32 MB PSRAM of the XIPHOS-X4. For maximum memory and robustness, the XIPHOS-X4 variant offers both encapsulation and external PSRAM.

13 XIPHOS-X4

13.1 Description

The XIPHOS-X4 is the **top-tier variant**: Phantom Forge® encapsulation, **32 MB** external PSRAM, and a maximum operating temperature of **140 °C**. It combines the environmental and mechanical robustness of the XIPHOS-X3 with the memory capacity of the XIPHOS-X2, making it suitable for the **most demanding industrial applications**: edge processing, high-throughput data handling, complex protocol stacks, and long data buffers in harsh or outdoor-like environments. The XIPHOS-X4 offers the **highest thermal**

margin and the **largest memory footprint** in the family while retaining the same electrical interface and software baseline as the other variants.

13.2 Key specifications

The key parameters for this variant are summarised below. Table 7 lists the main specifications for the XIPHOS-X4, the top-tier variant with encapsulation, 32 MB PSRAM, and 140 °C rating.

Parameter	Value
STM32 MCU	STM32H735IGT
MCU Flash (internal)	1 MB (ECC)
MCU SRAM (internal)	~564 KB
PSRAM (external)	32 MB
Flash (external)	8 MB
Lattice FPGA	ICE40UP5K-SG48I
Min temperature	-40 °C
Max temperature	140 °C

Table 7: Key specifications for XIPHOS-X4.

13.3 Notes

XIPHOS-X4 offers the highest thermal margin and expanded memory for advanced industrial applications, edge processing, and high-throughput data handling. It is the preferred choice when both environmental robustness (Phantom Forge®, IP66) and large RAM capacity are required, and when the application justifies the additional cost over the XIPHOS-X2 or XIPHOS-X3. The same carrier board and software stack can be used across XIPHOS-X1–XIPHOS-X4, allowing a single design to cover a range of environmental and memory requirements.

14 Operating conditions

XIPHOS modules are specified for industrial environments where thermal, mechanical, and electrical stress are higher than in typical commercial applications. All variants support an operating temperature range starting at **-40 °C**; the upper limit depends on the variant (**85 °C** for XIPHOS-X1, **125 °C** for XIPHOS-X2, and **140 °C** for XIPHOS-X3 and XIPHOS-X4). These limits assume that the module is used within the specified supply and interface conditions and that adequate cooling or thermal coupling is provided when the system runs at high load for extended periods.

In applications with high ambient temperature or limited airflow, thermal design of the carrier and enclosure is critical. The open-frame variants (XIPHOS-X1, XIPHOS-X2) rely on the end product to provide mechanical protection and, where needed, environmental sealing; the Phantom Forge® variants (XIPHOS-X3, XIPHOS-X4) offer improved resistance to humidity and contamination and are better suited to harsh or outdoor-like conditions. Condensation should be avoided on unencapsulated assemblies; in high-humidity or wash-down scenarios, the encapsulated versions are recommended.

EMC performance depends on the full system: PCB layout, enclosure, cables, and software. When integrating high-speed I/O (Ethernet, USB, etc.), follow controlled-impedance routing and grounding practices and validate emissions and immunity at the system level.

14.1 General operating notes

- Ensure adequate airflow or thermal coupling for sustained high load.
- Avoid condensation; use Phantom Forge® variants in harsh humidity.
- Validate EMC behavior at system level when integrating high-speed I/O.

14.2 Compliance and disposal

The product line has passed **CE marking** homologation and includes certifications for vibration and temperature. **All XIPHOS models are RoHS free.** Encapsulated variants (XIPHOS-X3, XIPHOS-X4) are rated to **IP66** for ingress protection, making them suitable for demanding industrial or outdoor installations where dust and water exposure are a concern.

Do not dispose of this equipment with household waste. Electronic assemblies must be handled through controlled waste management and delivered to an appropriate electronics recycling container or authorized collection point.

Environmental limits (temperature, humidity, mechanical shock) should be validated at the system level, including enclosure thermal behavior, airflow, and connector selection.

15 Electrical specifications

XIPHOS modules are designed to be powered from a single **5 V** supply provided by the carrier board through the board-to-board connectors. All internal regulation (e.g. for the MCU and FPGA core voltages) is handled on-module, so the system integrator only needs to provide a stable 5 V rail within the specified current range. This simplifies carrier design and avoids multiple external regulators.

15.1 Input supply

The module accepts a nominal input voltage of 5 V. The minimum current figure corresponds to a lightly loaded state (e.g. MCU in low-power mode with the FPGA unconfigured or idle); the maximum current covers full operation with MCU and FPGA active, Ethernet and USB in use, and typical I/O switching. The exact consumption depends on clock rates, peripheral usage, and FPGA bitstream. For margin in the end application, plan for the maximum current and ensure the 5 V source can sustain it without excessive droop. The main electrical limits are given in Table 8.

Parameter	Value
Input voltage	5 V
Minimum current	19 mA
Maximum current	280 mA

Table 8: Input supply specifications.

15.2 Power states

Different power states (e.g. standby, run with MCU only, run with MCU and FPGA) are available to balance performance and consumption. Exact current and wake-up behaviour for each state are documented in the product-specific datasheet or application notes. Power profiling should be performed in the target system to account for peripheral load, external transceivers, and connector configuration. Table 9 summarises the main power states.

State	Current
Standby	TBD
Run (MCU)	TBD
Run (MCU + FPGA)	TBD

Table 9: Power states (typical current).

15.3 Design recommendations

For power integrity on the carrier board, place low-ESR decoupling capacitors close to the connector power pins and maintain a solid ground reference. Use wide traces or planes for 5 V distribution to reduce voltage droop during peak load and to minimise EMI. High-speed signals (Ethernet, USB, clocks) should be routed with controlled impedance and kept away from power paths where possible.

16 Mechanical specifications

The mechanical form factor of XIPHOS is common to all variants: a compact module with a nominal PCB size of 55 mm × 40 mm and two connector strips along one or two edges for attachment to the carrier board. Dimensions, tolerances, keepout zones, and connector positions are detailed in the Mechanical Datasheet and the XIPHOS product page (downloads). Here we summarise the main differences between open-frame and encapsulated variants.

16.1 XIPHOS-X1 / XIPHOS-X2 (no Phantom Forge®)

The XIPHOS-X1 and XIPHOS-X2 variants are supplied as open-frame PCB assemblies: the MCU, FPGA, memories, and passives are mounted on the board, but there is no overmould or enclosure on the module itself. These versions are intended for integration into protected enclosures or carrier boards that provide mechanical support, thermal management, and environmental shielding. They are suited to cost-sensitive or space-constrained applications where the end product already provides the required protection.

- PCB dimensions: 55 mm × 40 mm
- Maximum component height: see mechanical datasheet (TBD)
- Connectors: two strips for power, ground, and signals (SPI, I^2C, Ethernet, USB, CAN FD, etc.)

16.2 XIPHOS-X3 / XIPHOS-X4 (with Phantom Forge®)

The XIPHOS-X3 and XIPHOS-X4 variants are encapsulated using Phantom Forge® technology, which adds a protective layer over the assembly, improves resistance to humidity and contamination, and can enhance mechanical damping in high-vibration environments. Encapsulated versions are recommended for harsh industrial or outdoor-like installations where open-frame boards would be at risk. The external dimensions remain 55 mm × 40 mm at the PCB level; the encapsulant may add a small amount to the overall stack height. Thermal anchor points and protection ratings are given in the mechanical document.

- Encapsulated dimensions: 55 mm × 40 mm (PCB); overall TBD
- Thermal anchor points: see mechanical datasheet (TBD)
- Protection rating: IP66 for encapsulated variants

When using Phantom Forge® variants, allow for adequate thermal coupling to the carrier or chassis to maximise heat transfer in high-temperature conditions, and follow the mounting and keepout guidelines in the mechanical datasheet.

17 Revision history

Document changes are recorded in the following table.

Table 10: Revision history.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of model-level structure.
v1.0	2025-02-02	Release 1.0 for distribution.
v1.1	2026-01-26	Official pinout diagram embedded; pinout section updated.

18 Disclaimer

This document is released as version 1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Electronics website and the XIPHOS product page (downloads). REIDITE Electronics reserves the right to make changes without notice.