REIDITE ELECTRONICS

XIPHOS Series

User Manual

Getting started, hardware setup, and software programming

v1.0

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STMicroelectronics

LATTICE SEMICONDUCTOR

1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2025-02-02	Release 1.0 for distribution.
v1.1	2026-01-26	Pinout updated from official diagram; diagram embedded in Models datasheet; new Pinout reference document added.

2 Hardware version guide

This documentation applies to XIPHOS hardware version **3.2.0**. Ensure that your module and carrier design match this revision; for other hardware versions, contact REIDITE Electronics or refer to the XIPHOS product page (downloads).

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3 Getting started

This manual describes how to use the XIPHOS System-on-Module (SoM) in your application. It complements the *XIPHOS Family Datasheet*, the *XIPHOS Models Datasheet*, and the *XIPHOS Mechanical Datasheet*, which contain electrical, mechanical, and model-specific specifications.

3.1 What you need

Before integrating a XIPHOS module, ensure you have:

- A XIPHOS module (XIPHOS-X1, XIPHOS-X2, XIPHOS-X3, or XIPHOS-X4) and its datasheets.
- A carrier board designed for the XIPHOS pinout, or the mechanical and electrical drawings to design one.
- A **5 V** power supply capable of delivering at least the maximum current specified for your variant (see the Models Datasheet).
- Mating connectors (Hirose FX11LA-100/10 or equivalent) on the carrier board, correctly placed according to the mechanical documentation.
- For software development: a debug probe (ST-LINK, J-Link, or compatible) and the recommended toolchain (STM32CubeIDE, GCC ARM, Lattice Radiant or iCEcube2 for the FPGA).

3.2 Document set

- **Family Datasheet** — Overview, architecture, features, applications, and ordering.
- **Models Datasheet** — MCU/FPGA details, pinout, electrical and operating conditions, and model comparison.
- **Mechanical Datasheet** — Board outline, connector placement, mounting holes, stack height, and tolerances.
- **User Manual** (this document) — Step-by-step hardware setup, software programming, connector usage, and troubleshooting.
- **Pinout Reference** — Connector pinout diagram (J1/J2).

All documents can be downloaded from the XIPHOS product page (downloads).

All XIPHOS modules are **RoHS free**. For compliance and disposal information, see the Models Datasheet.

4 Hardware setup

4.1 Unpacking and handling

1. Remove the module from its packaging in an ESD-safe area. Use a grounded wrist strap or work surface when handling the module.
2. Do not touch the connector pins or exposed components. Hold the module by the edges and avoid the connector mating area.
3. Check the module label to confirm the variant (XIPHOS-X1, XIPHOS-X2, XIPHOS-X3, or XIPHOS-X4) and that it matches your carrier design.

4.2 Installing the module on the carrier board

1. Ensure the carrier board is powered off and that the 5 V supply is disconnected.
2. Align the module connectors (J1 and J2) with the mating connectors on the carrier board. Refer to the Mechanical Datasheet for connector positions, orientation, and stack height.

3. Press the module firmly and evenly onto the carrier connectors until both connectors are fully seated. Do not apply excessive force or press on one side only; this can damage the connectors or the PCB.
4. Verify that the module sits flat and that there is no visible gap between the module and the carrier at the connector area.

4.3 Power connection

1. Connect the carrier board to a stable **5 V** supply within the specified voltage and current limits (see the Models Datasheet, Electrical specifications).
2. Apply power. The module does not have a separate power switch; power is controlled by the carrier board supply.
3. If the system does not start as expected, see 7 (Troubleshooting).

4.4 Phantom Forge® variants (XIPHOS-X3, XIPHOS-X4)

Encapsulated variants (XIPHOS-X3, XIPHOS-X4) have the same connector positions and pinout as open-frame variants. Installation and power steps are identical. The encapsulation improves resistance to humidity, dust, and mechanical stress; it does not change the electrical or software interface.

5 Software and programming

5.1 Development toolchain

- **MCU:** STM32CubeIDE or STM32CubeMX for project setup; GCC ARM and GDB for building and debugging. Use ST-LINK, J-Link, or OpenOCD for SWD/JTAG.
- **FPGA:** Lattice Radiant or iCEcube2, or the open-source toolchain (Yosys, nextpnr, IceStorm). Program the FPGA via JTAG during development.
- **RTOS:** FreeRTOS and other RTOSes are commonly used; refer to the application notes for recommended configurations.

5.2 First-time programming (MCU)

1. Connect your debug probe (ST-LINK or J-Link) to the SWD/JTAG pins on the carrier board. Pin assignments are in the Models Datasheet (Pinout).
2. Power the system with 5 V.
3. Open your IDE (e.g. STM32CubeIDE), load or create a project for the STM32H735, and build the application.
4. Start a debug session and run or flash the firmware. The MCU internal Flash and optional external Flash can be programmed via the debugger.

5.3 First-time programming (FPGA)

1. Connect the JTAG lines from your programmer to the FPGA JTAG pins on the carrier (see Pinout).
2. Use Lattice Radiant, iCEcube2, or the IceStorm tools to build the bitstream and program the FPGA via JTAG.
3. For production, the bitstream is often stored in external Flash and loaded by the MCU at boot; see the Models Datasheet (Programming and debug) for details.

5.4 In-field updates

The MCU supports firmware updates without a debugger via the on-chip bootloader (USB-DFU, UART, or other configured interfaces). Place the device in bootloader mode (e.g. via GPIO or power-up sequence) and deliver the new image over the selected channel. FPGA updates can be performed by storing a new bitstream and having the MCU reconfigure the FPGA at boot or on command.

6 Connectors and carrier interface

6.1 Connector identification

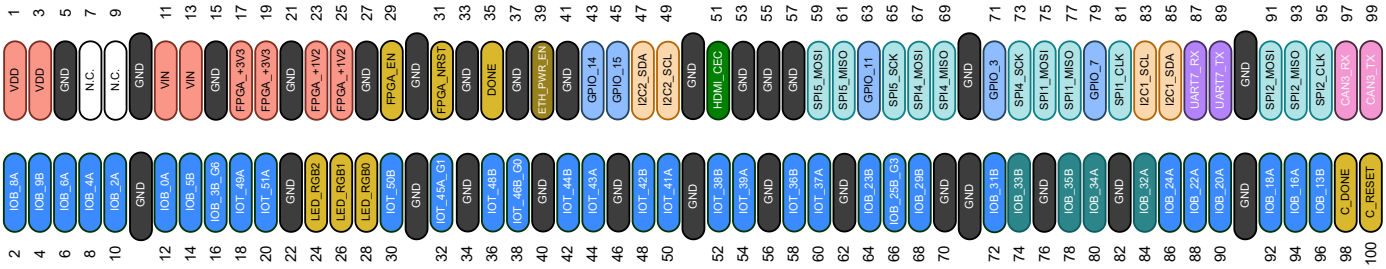
XIPHOS has two 100-pin board-to-board connectors:

- **J1** and **J2** — Hirose FX11LA-100/10 (or equivalent as specified in the mechanical documentation).
- They carry power, ground, and all digital and analogue signals (SPI, I²C, UART, GPIO, Ethernet, USB, CAN FD, FPGA I/O, debug).

The pinout is **identical across all variants** (XIPHOS-X1–XIPHOS-X4), so one carrier design can host any XIPHOS model.

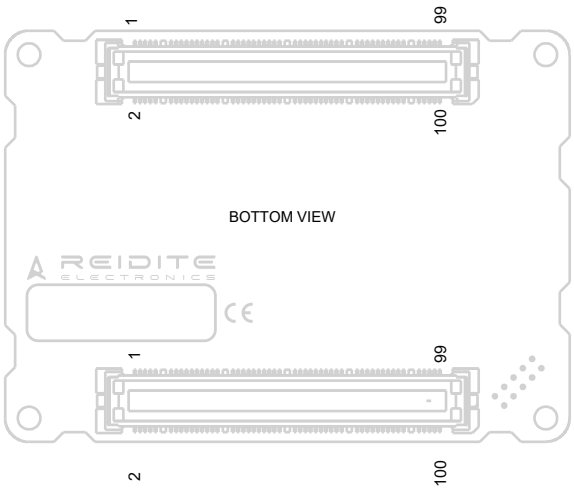
6.2 Pinout diagram

The connector pinout (J1 and J2) is shown on the following pages. Use it together with the *XIPHOS Models Datasheet* for detailed tables and alternate functions.



Leyenda:

- POWER
- STM Control
- FPGA Control
- Ethernet Control
- I/O STM
- I/O FPGA
- I/O Ethernet
- STM SPI
- FPGA SPI
- STM I2C
- FPGA I2C
- STM UART
- STM CAN
- STM USB
- STM SDMMC
- STM HDMI
- GND
- N.C. = Not Connected



Función

Pin | Principal | Alternativa

6.3 Using the pinout

1. Use the *XIPHOS Models Datasheet*, Pinout section, for the exact pin assignments and alternate functions.
2. Many pins are multiplexed; ensure your firmware or bitstream configures the correct function (e.g. UART vs GPIO).
3. Pins are not 5 V tolerant unless stated in the pinout. Do not exceed the MCU/FPGA I/O voltage.
4. For Ethernet, USB, and other high-speed signals, follow controlled-impedance routing and grounding guidelines on the carrier to meet EMC and signal integrity requirements.

6.4 Mating and unmating

- To **remove** the module: power off, then carefully lift the module straight up from both connectors. Do not twist or pull at an angle.
- Repeated mating/unmating can wear the connectors; minimise cycles if possible. Use the vendor-recommended mating connector and footprint on the carrier.

7 Troubleshooting

7.1 Module does not power up or show signs of life

- Check that the carrier supplies a stable **5 V** within the specified current capability and that polarity is correct.
- Verify that the module is fully seated on both connectors (J1 and J2).
- Inspect the connector area for bent pins, contamination, or damage.
- Confirm that the carrier board schematic matches the XIPHOS pinout (power and ground pins in particular).

7.2 Debugger cannot connect (MCU)

- Ensure SWD/JTAG lines (and VDD, GND if required by the probe) are correctly routed from the carrier to the debug connector.
- Check that no other driver or application is holding the debug interface (close other IDEs or tools).
- Try a power cycle: remove power, wait a few seconds, then reapply and retry the connection.
- If the MCU was set to disable the debug port, use the bootloader (e.g. USB-DFU or UART) to recover or re-enable debug access as per the product documentation.

7.3 FPGA does not configure

- Verify JTAG connectivity and that the correct voltage levels are used for the FPGA I/O.
- If the bitstream is loaded by the MCU at boot, ensure the MCU firmware has loaded the correct image and that the storage (e.g. Flash) is accessible and intact.
- Check the Models Datasheet for the recommended configuration flow (JTAG vs MCU-loaded).

7.4 Ethernet or other interfaces not working

- Confirm pin mapping and alternate function configuration in your firmware and carrier design.
- For Ethernet, ensure the PHY is powered and that RMII/RGMII (or applicable) signals are routed with correct impedance and length matching.

- Review the electrical and operating conditions; ensure the module is within the specified temperature and supply limits.

7.5 Where to get help

For further support, contact REIDITE Electronics with your module variant, carrier description, and a concise description of the symptom and steps already tried. Refer to the ordering section in the Family Datasheet for contact information.

8 Safety and warnings

8.1 Electrical safety

- Only use the module with the specified **5 V** supply. Incorrect voltage or polarity can damage the module and void the warranty.
- Do not open or modify encapsulated (Phantom Forge®) variants; the encapsulation is part of the product design and protection.
- Ensure the carrier board and any external circuitry are designed for safe operation and do not expose users to hazardous voltages or currents.

8.2 ESD and handling

- Handle the module in an ESD-safe environment. Use grounded wrist straps and work surfaces when appropriate.
- Store and transport the module in anti-static packaging when not installed.

8.3 Environment and disposal

- Operate the module within the specified temperature and humidity limits for your variant (see the Models Datasheet).
- **Do not dispose of this equipment with household waste.** Electronic assemblies must be recycled or delivered to an authorised collection point in accordance with local regulations.

8.4 Compliance

XIPHOS modules comply with applicable CE marking and are **RoHS free**. For full compliance and certification details, refer to the Family and Models Datasheets.

9 Revision history

Changes to this manual are summarised in the following table.

Table 1: Revision history.

Version	Date	Changes
v0.1	2025-01-22	Initial release of User Manual.
v1.0	2025-02-02	Release 1.0 for distribution.
v1.1	2026-01-26	Documentation update; pinout reference and new Pinout document.

10 Disclaimer

This document is released as version 1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Electronics website and the XIPHOS product page (downloads). For the latest specifications, always refer to the official datasheets and the REIDITE Electronics website.